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Design of low power, low noise instrumentation amplifiers for MEMS sensor interfacing

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Sommario

La presente tesi di dottorato tratta del progetto di amplificatori da strumentazione in tecnologia CMOS atti ad interfacciare sensori MEMS resistivi. Il progetto di un amplificatore da strumentazione a basso offset e basso rumore, utilizzato per la lettura di sensori di flusso MEMS, viene ampliamente discusso. Per raggiungere l'elevata risoluzione richiesta, sono state utilizzate tecniche dinamiche, come ad esempio la modulazione chopper e il matching dinamico delle porte di ingresso. La stretta banda di frequenze richiesta dall'applicazione viene ottenuta implementando nell'amplificatore stesso un filtaggio passa-basso del secondo ordine. Sono inoltre stati forniti dei criteri per la progettazione ottima di filtri a bassa frequenza.
Infine, viene presentato il progetto di un amplificatore da strumentazione per sensori magnetici integrati, sviluppato presso NXP Semiconductors (NL), durante una internship di 8 mesi, svolta all'interno del Programma di Dottorato.

Abstract

This Ph.D. thesis deals with the design of CMOS instrumentation amplifier for resistive MEMS sensor interfacing. The design of a low-offset, low-noise instrumentation amplifier, targeted to the read-out of MEMS thermal flow sensors, is presented. To achieve the high resolution required, dynamic techniques such as chopper modulation, dynamic element matching and port-swapping have been used. The narrow bandwidth required for this applications has been obtained implementing in the amplifier block also a second order filtering function. Optimum design criteria for low-frequency filter optimization have been developed and are also reported.
Finally, the design of an high gain-matching multi-channel instrumentation amplifier for integrated magnetic sensors, carried out during an internship at NXP Semiconductors, has been discussed.

Contents

Introduction

In the last decade MEMS market has faced a fast growth and an even faster pace is expected in the next years, with double-digit market expansion. While MEMS success is mainly due to inertial sensors, like accelerometers and gyroscopes, several new classes of integrated sensors and systems have been developed throughout the years.
Among them, silicon integrated gas flow meters are becoming interesting also from a commercial point of view, after an initial research phase. With respect to their traditional, macroscopic counterpart, they offer better performances, faster response and minor costs and power consumption thanks to the minimization. Moreover, processing techniques fully compatible with CMOS processes have been developed to fabricate this kind of sensor. This factor enabled the integration of the sensor and the electronic interface on the same chip. Besides the silicon area saving, this approach greatly reduces the interferences and disturbances coming from the environment, reduces the parasitics associated with pads and connections and reduces the costs.
Among the others, flow meters employing thermal transducers, such as heaters and thermopiles, represent the largest fraction, thanks to their high performances and easiness of integration. Since the output signal of this kind of sensors is a differential voltage in the mV range, high precision electronic interfaces are required to preserve the sensor dynamic range. Low-noise, low-offset, narrow bandwidth CMOS instrumentation amplifiers can be successfully used to interface integrated thermal flow sensors. To achieve the required µV resolution, it is necessary to adopt dynamic offset compensation techniques. Moreover, electronic noise has to be carefully controlled, trying at the same time to minimize the power consumption. At the same time, high input impedance amplifiers have to be designed, since thermal sensors often present an high se-

ries resistance. Gain accuracy is another critical requirement.
In this thesis a novel instrumentation amplifier, employing chopper modulation, dynamic element matching and input-impedance boosting by means of a port-swapping approach is presented. The amplifier has been targeted to interface integrated flow sensors with series resistances ranging from 10 to a few hundreds of kΩ. An optimum trade-off between noise and power consumption has been searched. The amplifier is also capable of a low-frequency filtering, in order to limit the system output noise bandwidth.
In **Chapter 1** MEMS thermal flow sensors principle of operation and fabrication process are shown. In **Chapter 2**, dynamic offset compensation techniques are reviewed. In **Chapter 3** several examples of high precision instrumentation amplifier found in the literature are discussed as possible approaches to interface MEMS thermal sensors. In **Chapter 4** the instrumentation amplifier is presented. The principle of operation is discussed, as well as the techniques employed to enhance its performances. The schematic design is reported, together with simulation results useful to prove the efficiency of the proposed solution. In **Chapter chap:soc** the layout of the proposed interface is briefly reviewed and its integration with other building blocks and the target flow sensors on a single chip are shown. In **Chapter 6** the problem of minimizing the area of G_mC integrators, often used as basic building blocks of low-frequency filters, is discussed. A MATLAB routine, capable of automatic sizing and optimization of G_mC integrators is also presented. Several design hints obtained from this study have been employed to optimally sizing the instrumentation amplifier.
Finally, in **Chapter 7** the results of a research activity carried out at NXP Central R&D, Eindhoven (NL), have been reported. The design of an instrumentation amplifier for magnetic sensors interfacing, characterized by an extremely high channel-gain matching, obtained with a very small silicon area, is shown.

Chapter 1

MEMS flow sensors

In the last decade MEMS market has faced an outstanding, double-digit growth, and is exptected to expand at the same high rate also in the next years. In addition to traditional inertial MEMS sensors, several different devices have been developed. Among the others, MEMS thermal flow sensors promise to become a strong alternative to traditional flow sensors, thanks to thier unprecedented performances, such as wide measurement range, low power consumption and miniaturization. In this chapter thermally based CMOS flow sensors will be briefly introduced. Their principle of operation, as well the fabrication technology, will be discussed.

1.1 MEMS and microsensor market

In the past decade MEMS and microsensor based applications have experienced a double-digit growth and will see a continuous growth for the next years, with a rate ranging from 10 % to 20 %, as shown in Fig. 1.1.

This outstanding growth has been enabled by several unique characteristics of MEMS, such as the small dimensions, high accuracy, low sensitivity to external disturbance thanks to their high level of integration, and batch production. Nowadays the applications of MEMS technology are widespread: accelerometers and gyroscopes for positioning, motion sensing and navigation in auomotive, entertainment and mobile fields, dense micromirrors for high-definition optical displays, pressure sensors, flow sensors, infrared detectors, magnetic sensors. Potential medical applications are arising, such as microp-

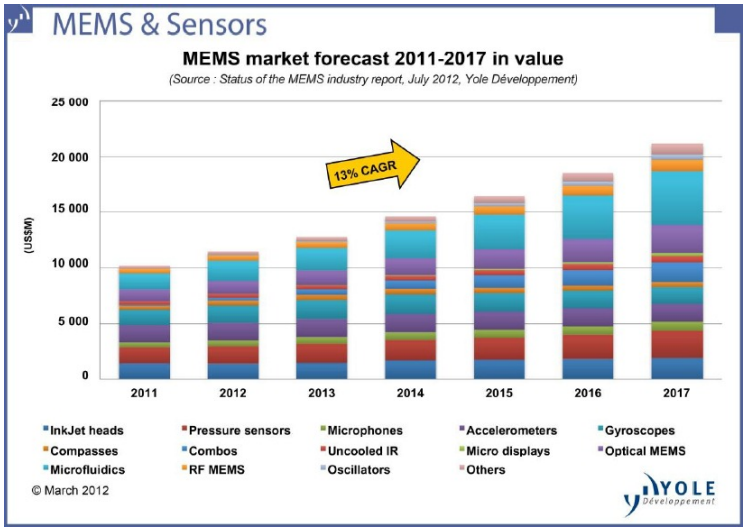

Figure 1.1: MEMS market value from 2011 to 2017 [1.1].

umps for controlled drug delivery. The integration of lab-on-chip for chemical or biological analysis is also a promising field.
MEMS technology has initially developed from IC standard processes, such as litography, epitaxy, selective etching and so on, but has also driven the development of MEMS-specific technologies, such as the Deep Reactive Ion Etching (DRIE) in order to enlarge the field of applications or increase the performances. The possibility to integrate CMOS-compatible MEMS or microsensors has also enabled the possibility of integrating the mechanical or sensing part along with the electronic interface on the same die, realizing the so-called System-on-Chip (SoC), with advantages in terms of package size, robustness to interferences and power consumption [1.2].

1.2 MEMS CMOS thermal sensors

Integrated MEMS thermal sensors [1.3] use a thermal transduction to directly measure temperature or indirectly measure a quantity of interest. This temperature variation is then converted into an electrical signal. The small size of integrated thermal sensor systems reduces the time constants of the thermal effect, making them practical for measuring diverse physical quantities. The CMOS compatibility should be guaranteed in order to minimize the sensor system size, power consumption and to make easier the reading of very small output signals, thanks to the merging of the electronics and micromachined sensor on the same chip.

CMOS compatible thermal microsensors are fabricated starting from a CMOS layout with additional post-processing steps, such as removal of thermally conducting material for isolation of heated structures. Post-processing approach includes wet and dry silicon etching, either iso or anisotropic, for bulk or surface micromachining, metal or dioxide deposition, patterning [1.4]. Particular care has to be taken in performing CMOS post processing steps. As an example, a temperature exceeding 400°C can destroy the metallization, thus low temperature processes have to be used to deposit high-quality thin films. Also the introduction of mechanical stress can degrade the performances of the CMOS components. Finally, packaging is not straigthforward and often requires the invention of new application-specific solutions [1.5, 1.6, 1.7].
CMOS-based thermal sensors are used in a large variety of applications and use different sensing principles. One of the most popular approaches is the integration of thermopiles [1.8] on the chip surface, since metal, polysilicon and diffused bulk silicon can all serve as thermocouple materials [1.3], thanks to their different Seebeck coefficients. This approach has been used for the fabrication of infrared detectors [1.9, 1.10], anemometers [1.11, 1.12, 1.13], flow sensors [1.14, 1.15, 1.16]. Alternative approaches have also been extensively evaluated. In [1.17], Tezcan, Eminoglu and Akin propose an uncooled CMOS-based microbolometer integrated used a commercial 0.8 µm CMOS process. The selected infrared sensitive element is a suspended n-well layer. In [1.18], Wang and Lu propose an array of miniaturized CMOS thermal sensors, measuring the heat produced by glucose oxidation evaluating the source-to-drain current of p-type sensing transistors. This approach is proposed to overcome the limited sensitivity of CMOS thermopile sensors, not high enough for the application.

1.3 MEMS flow sensors

A large variety of conventional flow sensors is used in the industry for gas or liquid flow monitoring, process control and so on. However, they suffer from low sensitivity, large size and interfacing difficulties. Microfabricated flow sensors can overcome these issues, thanks to their small size, fast response, integrated signal processing and low cost. Recently, important firms as Sensirion AG, Honeywell, Bosch, brought microfabricated flow sensors from research stage to industrial production.
In spite of the crisis the automotive market is facing in the last years, integrated electronics and sensor content in a car is continuosly increasing [1.19, 1.20]. In

this field, micromachined flow sensors have found application in the injection system, to measure the air sucked into the cylinder. Other widespread applications are wind measurement [1.12, 1.13], transport and process industry, medication and surgical tools [1.21], climate control and many others, including also systems working in extreme environments like space.
The necessity of defining microchannels to be used as proper interfaces between fluids and the integrated flow sensor, the flow regime, either laminar or turbolent, the intrinsecal difficulties arising when dealing with fluidodynamics and the availability of different sensing principles make the realization of effective flow sensors quite complex.

1.3.1 MEMS thermal flow sensors

The largest fraction of the above cited flow sensors works in the thermal domain. It has been also widely proven that high performance sensors can be fabricated starting from standard CMOS integrated circuit process and adding some post-processing steps, as described above. In order to allow the CMOS compatibility, the sensor design and fabrication should respect the followings [1.3]:

- use of CMOS IC materials.
- exploitation of thermal effects inherent to CMOS materials.
- designed structures should bring out the transducer effects within the limits of the CMOS post-processing, cited in Sec. 1.2

CMOS materials clearly include bulk silicon, polysilicon (n- and p-type), dielectrics and metal. Metal and silicon conduct heat efficiently. Unfortunately, dielectric layers cannot provide a good enough isolation. Therefore, the removal of bulk silicon is used to achieve the necessary thermal isolation. The thermoresistive effect (Joule effect) can be used for resistive heating in hot wire anemometers, while the difference in thermopower between CMOS conducting materials can be exploited to integrate thermocouples and thermopiles, used in calorimetric flow sensors, as described later in this section.
As stated before, thermal flow meters exploit the heat transfer due to a mass flow. They can be usually classified in three groups [1.22]:

- hot wire/hot film anemometers
- time of flight sensors
- calorimetric sensors

Hot wire anemometers generally consist of a single heated element and the fluid flow influence on this element is measured. Their principle of operation is sketched in Fig. 1.2. Usually, the power W dissipated on the anemometer

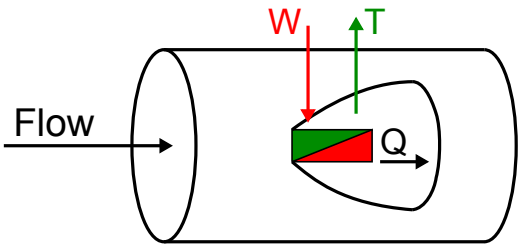

Figure 1.2: Principle of operation of an hot wire anemometer.

is kept constant, while heat Q is dissipated into the flow. The temperature T is a measure of the flow. A decrease of T is observed when the fluid flow increases. An alternative approach is the constant temperature mode. In this configuration heater temperature is kept constant and the power spent to do it is the measure of the flow. The measurement results to be very fast, but an additional control system is necessary. In both cases, the anemometer is based on the King's law:

$$G_T(v) = G_T(0)\sqrt{1+\beta_v} \tag{1.1}$$

where $G_T(v)$ is the total thermal conductance seen by the wire (film), which depends on the flow velocity v. The empirically determined coefficient β depends on the fluid characteristics and sensor geometry. Usually, integrated anemometer are realized by means of a dielectric cantilever (hot wire) or membrane (hot film) and a patterned layer of platinum, but also more complicated structure have been described [1.23]. Although other materials can be used, platinum offers the best chemical stability with temperature. The wire is driven to a temperature higher than the fluid temperature to enable the correct heat flow. Moreover, the T variation also influences the electrical conductivity of the film, offering the possibility to detect velocity through this variation. Hot wire anemometers have typically a limited lower range due to convection and are not sensitive to flow direction. The wires are kept very thin in order to increase the response speed, at cost of increased fragility.

In time of flight flow sensors (Fig. 1.3) an heater is continually pulsed with a certain amount of power. The fluid flow carries heat away from the heater, towards a temperature sensor. By measuring the time delay between the pulse and the temperature variation revealed by the sensor, it is possible to measure the fluid flow velocity. Thus, at minimum two wires are necessary. Another

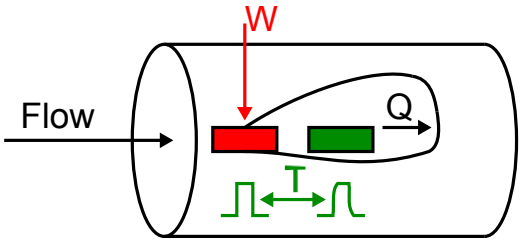

Figure 1.3: Principle of operation of a time of flight sensor.

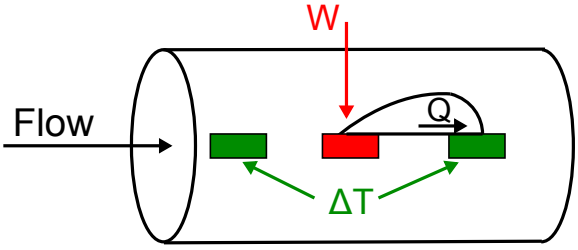

Figure 1.4: Principle of operation of a calorimetric flow sensor.

wire can be added in order to make the sensor bidirectional. This kind of sensors is best suited to work in large fluid velocity conditions. In this condition, the heat pulse shape is not deformed due to diffusion. The measurement range is defined by the distance between heater and sensor. Although this approach is not often used in thermal flow sensors, in [1.22], a time of flight flow sensor is proposed.

Finally, Fig. 1.4 shows the principle of operation of a calorimetric flow sensor. Although a calorimetric flow sensor can be built with an heater and a single temperature transducer, most of the sensors of this kind use up- and downstream temperature sensing elements, in order to render the sensor bidirectional. As shown in Fig. 1.4, the downstream sensor is heated, due to the heat carried by the flow, while the upstream sensor is cooled. The difference of temperature is then dependent on the flow rate. Calorimetric flow sensors are characterized by an higher sensitivity than anemometers [1.24] and are well suited for measuring low flow rates. In [1.12] an anemometer exploiting the calorimetric principle is presented. The temperature transducers are implemented with integrated thermopiles. In the following section a CMOS calorimetric flow sensor is presented.

1.4 CMOS integrated calorimetric flow meters

In this section the principle of operation and fabrication process of a CMOS calorimetric flow meter is briefly described. The sensor has been developed in the "Dipartimento di Ingegneria dell'Informazione" of University of Pisa and consists in a double heater structure, with n+/p+ polysilicon thermopiles.

1.4.1 Principle of operations

To understand the principle of operation of the calorimetric sensor it is possible to make reference to the single heater structure represented in Fig. 1.5. The

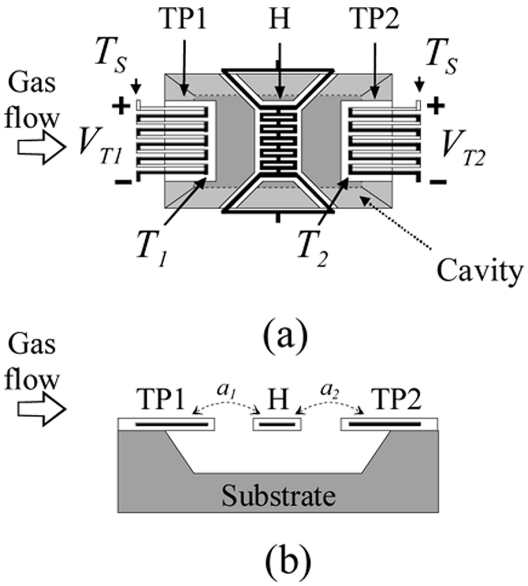

Figure 1.5: Layout of a single heater sensor: (a) plan view and (b) cross section (not to scale). Thermal coupling coefficients a_i are also represented, after [1.25] (© [2011] IEEE).

sensor consists in an heater H and two thermopiles TP1 and TP2. The hot junctions are thermally insulated from the substrate and their temperatures are indicated with T_1 and T_2, respectively. The cold junctions are placed onto the silicon substrate and can be considered isothermal. The voltages V_{T1} and V_{T2} produced by the two thermopiles are given by:

$$V_{T1} = s_1 (T_1 - T_S) \tag{1.2}$$

$$V_{T2} = s_2 (T_2 - T_S) \tag{1.3}$$

where T_S is the substrate temperature and s_1 and s_2 are the Seebeck coefficients of the two thermopiles. Hypothesizing that i) heat transport occurring by conduction or forced convection, ii) the inlet flow is at the same temperature of the substrate, and iii) the flow properties are constant, it can be shown that there is a linear relationship between the power of the heat sources and all temperature differences with respect to the substrate. Indicating the heater power with W, it is possible to write:

$$T_1 - T_S = W \cdot a_1(Q) \tag{1.4}$$

$$T_2 - T_S = W \cdot a_2(Q) \tag{1.5}$$

where $a_1(Q)$ and $a_2(Q)$ are thermal coupling coefficients depending on the fluid flow Q. Then, the output voltage V_{out} results to be given by:

$$V_{out} = V_{T2} - V_{T1} = W\left[s_2 a_2(Q) - s_1 a_1(Q)\right] \tag{1.6}$$

When a flow is present, the coefficient a_2 increases while a_1 decreases, or vice versa if the fluid flows in the opposite direction. Tipically, $s_2 = s_1 = s$, then:

$$V_{out} = Ws(a_2 - a_1) \equiv f(Q)Ws \tag{1.7}$$

where $f(Q)$ is a function of the flow rate. With a first order approximation we obtain:

$$V_{out} = f(0)Ws + \beta Ws \cdot Q \tag{1.8}$$

where $\beta = \delta f/\delta Q$. For a detailed description of the sensing principle the reader can make reference to [1.26]. In an ideal structure $f(0) = 0$ for symmetry reasons. The sensor sensitivy S is defined as:

$$S = \frac{\partial V_{out}}{\partial Q} = \beta Ws \tag{1.9}$$

The sensitivity of this kind of calorimetric sensors ranges from 100 to 1000 µV/sccm [1.26]. The sensor output is usually linear only for small flow rates. The typical output voltage is then a differential voltage in the order of a few mV, with a common mode given by the voltage applied at the lower end of the thermopile.
A problem affecting micrometric mass flow sensor is the dependence of S on the gas pressure. This problem has been addressed in [1.25].
The resolution, defined as the minimum variation of the input flow rate that

can be detected, is given in terms of the equivalent noise flow rate, $Q_{np-p} = v_{np-p}/S$, where v_{np-p} is the peak-to-peak amplitude of the total output noise voltage. The latter can be calculated assuming that, for Gaussian noise, $v_{np-p} = 4v_{nrms}$. The sensor noise is essentially associated with the resistance R of the thermopiles. Then:

$$v_{np-p} = 4\sqrt{4kTRB} \tag{1.10}$$

where k is the Bolztmann constant, T is the absolute temperature and R is the thermopile resistance, dependent on the used materials and the physical dimensions and ranges from tens of kΩ to a few MΩ. The bandwidth B is extended from DC to a few hundred of Hz. Usually, T is taken as the room temperature, as the thermopile temperature is generally overheated to a few Kelvin over it. Typical values for Q_{np-p} are in the range of $1 \cdot 10^{-3}$ sccm. A full scale flow rate Q_{max} can also be defined, as the sensitivy drops at high flow rates, due to several factors. Then, the sensor dynamic range DR can be defined as:

$$DR = \frac{Q_{max}}{Q_{np-p}} \tag{1.11}$$

and indicates the number of distinct flow levels distinguished by the sensor. This figure of merit is particularly important when dealing with high flow rates to be measured with great accuracy. The DR of macroscopic flow sensor is tipically in the order of 10^2, whereas MEMS flow sensors can easily achieve a DR of around 10^3.

The single heater flow sensor described above present a significant issue: due to unavodidable asymmetries of the sensing structure, such as geometry or material properties, $f(0) \neq 0$ and an intrinsic offset is originated. The offset is typically much larger than the sensor resolution, and seriously limits the possibility of detecting small fluid flows. The significant offset temperature drift and its dependence on gas properties also invalidates the standard offset compensation techniques. A double heater structure can be used to compensate for this offset. Fig. 1.6 shows the double-heater structure. The heater is split into two identical sections, driven by W_1 and W_2, which can be exploited to compensate for sensor offset. With the hypothesis of linear relationship between heater powers and thermopile overheating:

$$V_{T_1} = s_1 \left(W_1 a_{1,1} + W_2 a_{1,2}\right) \tag{1.12}$$

$$V_{T_2} = s_2 \left(W_2 a_{2,2} + W_1 a_{2,1}\right) \tag{1.13}$$

where $a_{i,j}$ are the coupling coefficients, as in Eq. 1.5. Thus:

$$V_{out} = W_2 \left(s_2 a_{2,2} - s_1 a_{1,2}\right) - W_1 \left(s_1 a_{1,1} - s_2 a_{2,1}\right) \tag{1.14}$$

The response to a gas flow is similar to the single heater structure. If a flow is present as in Fig. 1.6 $a_{2,2}$ and $a_{2,1}$ increase, while $a_{1,1}$ and $a_{1,2}$ decrease, producing a positive voltage. Since in a symmetrical structure $s_1 = s_2$, $a_{2,2}(0) = a_{1,1}(0)$ and $a_{1,2}(0) = a_{2,1}(0)$, if the heater are driven with $W_1 = W_2$ the offset voltage would be zero. With a proper unbalance, $W_1 \neq W_2$, the offset in real devices can be cancelled:

$$\frac{W_1}{W_2} = \frac{\left(s_1 a_{1,1}(0) - s_2 a_{2,1}(0)\right)}{\left(s_2 a_{2,2}(0) - s_1 a_{1,2}(0)\right)} \tag{1.15}$$

The heater can be driven with constant currents I_{H1} and I_{H2}, respectively. Eq. 1.15 becomes:

$$\frac{I_{H1}^2}{I_{H1}^2} \frac{\left(s_1 a_{1,1}(0) - s_2 a_{2,1}(0)\right)}{\left(s_2 a_{2,2}(0) - s_1 a_{1,2}(0)\right)} \tag{1.16}$$

where R_{H1} and R_{H2} are the electrical resistances of H1 and H2, respectively. The current ratio depends only on the ratio of homogeneous quantities. For

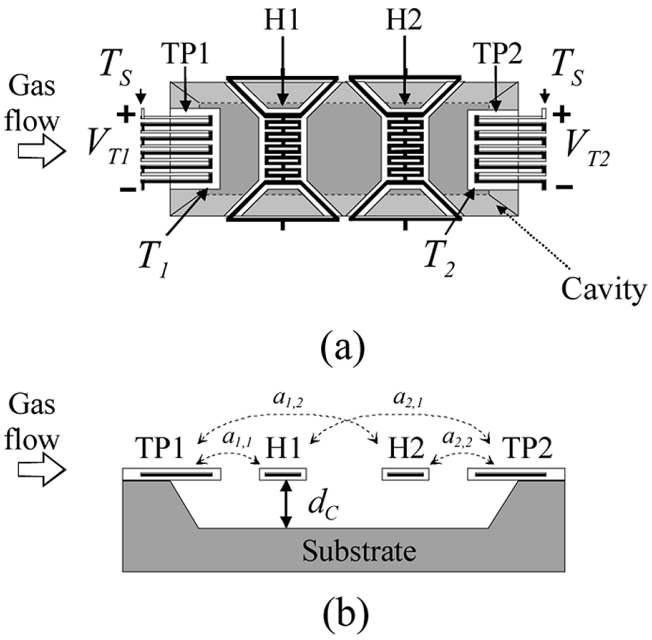

Figure 1.6: Layout of a single heater sensor: (a) plan view and (b) cross section (not to scale). Thermal coupling coefficients a_i are also represented, after [1.25] (© [2011] IEEE).

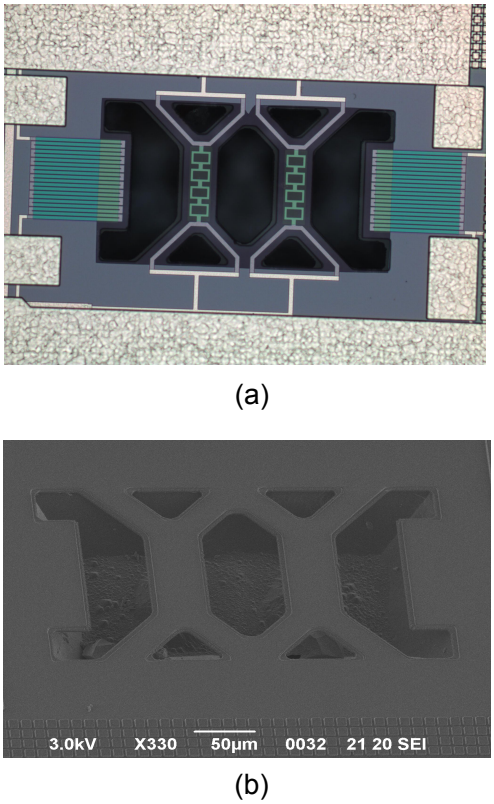

Figure 1.7: Optical microscope image (a) and SEM image (b) of an integrated calorimetric flow sensor.

this reason, this technique can be considered robust to temperature variations, at least at the first order [1.25].

1.4.2 Device fabrication

The described devices can be fabricated by means of postprocessing, consisting in applying simple and cheap steps to a CMOS structure, fabricated using commercial microelectronic processes. In the following the process used for fabricating the sensors described in [1.26] will be reviewed. The CMOS starting process was the BCD6s 3.3 V, 0.32 µm STMicroelectronics process. Fig. 1.7 shows an optical microscope image (a) and a scanning electron microscope (SEM) image of an integrated calorimetric flow sensor. Thermopiles and heaters can be easily identified in Fig. 1.7(a), while the 3D structure is shown in Fig. 1.7(b). The heaters are polysilicon resistors, placed over suspended dielectric membranes. The thermopiles consist of 10 n+/p+ polysilicon thermocouples with the hot

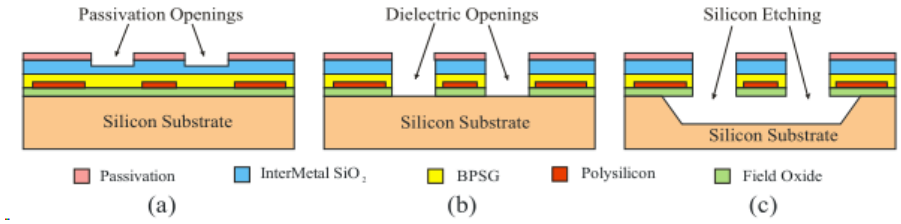

Figure 1.8: Schematic view of the post-processing steps: passivation openings as defined by the silicon foundry (a); dielectric openings by Reactive Ion Etching (RIE) (b); silicon etching in TMAH (c).

junctions placed on a cantilever beam. This material combination is often preferable [1.3, 1.11]. Typical thermopowers (Seebeck coefficients) are as high as some hundred µV/K, and ranges from 300 to 450 µV/K. The thermopiles used in [1.26] have a Seebeck coefficient of 315 µV/K and an internal resistance of 50 kΩ, which is in the CMOS thermopiles typical range, extended from few tens of kΩ to a few MΩ. The heaters and thermopile hot junctions have been insulated from the substrate by means of post-processing bulk-micromachining steps, schematically shown in Fig. 1.8. The dielectric layers have been selectively removed from the front-side to access the bulk silicon. Part of the passivation layer and of the inner-metal dielectric layers have been removed after the chip fabrication directly by the foundy (Fig. 1.8(a)), exploiting the same etching steps used for the chip pad definition. The remaining dielectric layers have been removed during post-processing by reactive ion etching (RIE) following a litographic step (Fig. 1.8(b)). Then, silicon anisotropic etch has been performed through the holes using an aqueous solution of TMAH, silicic acid and ammonium persulfate (Fig. 1.8(c)). The cavity depth is 80 µm. More details on the process can be found in [1.7].
After post-processing, the chip has been packaged in DIP28 ceramic cases, using a PMMA (poly-methyl-methacrylate) structure to convey multiple flows to different areas of the chip. [1.26].

1.5 Conclusions

In this chapter MEMS thermal sensors have been introduced as a promising approach to miniaturize several classes of sensors. Among them, MEMS thermal flow sensors guarantee higher performances than macroscopic sensors. The principle of operation of a calorimetric flow sensor has been reviewed, as well as the fabrication process. Since flow sensors represent the target application for the instrumentation amplifier proposed in this thesis, important specifications

have been pointed out, as the output voltage in the mV range and the internal series resistance in the order of tens of kΩ to a few MΩ.

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Chapter 2

Low offset amplifiers

Very low input offset level are mandatory when small amplitude DC signals have to be processed, as in the case of thermal sensor interfacing. In this chapter offset in CMOS circuits and dynamic techniques to reduce its impact will be reviewed. Time-domain sampling techniques such as Autozero and Correlated Double Sampling will be discussed, as well as frequency-domain continuous-time chopper modulation. Their effect on offset and noise will be analyzed, together with the non-idealities causing residual offset.

2.1 Offset in CMOS circuits

When a CMOS differential amplifier or a current mirror is designed, it is assumed that nominally identical devices have identical electrical characteristics and behaviour. In differential circuits this assumption leads to a perfect simmetry between the positive and negative sections, decreasing the offset voltage. On the other hand, current mirrors require the output current to be a perfect replica of the input. This is possible only if the devices of the circuit perfectly match. When the circuit is physically realized, however, small deviations of the MOS parameters, like the gate area or doping level, occur, due to uncertanties in the fabrication process. This leads to a mismatch between nominally identical transistors. Although errors on the absolute value of electrical parameters of integrated devices can reach also 30-40 % and vary a lot from a die to another, usually the matching error between close devices on the same chip is limited to a few percent, since they have very similar values of the physical parameters (oxide thickness, effective dimensions, doping level).

2.1.1 Offset modelling

The matching errors can be divided into systematic and random. The former is usually related to layout or design errors. Random errors are usually described by a Gaussian distribution and characterized by the standard deviation σ and depend mainly on random fabrication uncertanties. Taking into account the MOS drain current equation:

$$I_d = \frac{\beta}{2}\left(V_{GS} - V_{TH}\right)^2 \tag{2.1}$$

we can distinguish two sources of error: β and V_{TH}. If two MOS transistors are matched, the standard deviation of these quantities is given by the Pelgrom relationship [2.1]:

$$\sigma_{\Delta V_{TH}} = \frac{c_{VTH}}{\sqrt{WL}} \tag{2.2}$$

$$\sigma_{\Delta\beta/\beta} = \frac{c_{\beta}}{\sqrt{WL}} \tag{2.3}$$

where c_{VTH} and c_{β} are proportionality coefficients dependent on the technological process. Typical values for c_{VTH} are in the order of 5 mVµm and of $5 \cdot 10^{-3}$ µm for c_{β}. It is important to note that the deviation of the parameters scales down with the square root of gate area. This means that minimizing offset leads to a large silicon area. However, increasing the area of the devices is not enough, since this relationship holds as long as proper layout for matched devices is carried out. Layout techniques such as identical devices, same orientation, close positioning, interdigitation or common centroid, dummy devices are mandatory to obtain low offset level. A comprehensive description of these techniques can be found in [2.2].

2.1.2 Offset in current mirrors and differential amplifiers

To gain a better view on how the mismatch reflects on offset, it is possible to report two examples: the current mirror and the differential amplifier with resistive load. Fig. 2.1 shows a current mirror with unitary gain. Since the gain is 1, $\beta_1 = \beta_2$. Due to matching errors, this relationship does not hold, and also a difference of V_{TH} is present between M_1 and M_2. Indicating with I the average current flowing into the devices and with ΔI $I_1 - I_{out}$, it is easy to show that:

$$\frac{\Delta I}{I} = \frac{\Delta\beta}{\beta} - 2\frac{2\Delta_{VTH}}{(V_{GS} - V_{TH})} \tag{2.4}$$

Calculating the standard deviation we obtain:

$$\sigma_{\Delta I/I} = \sqrt{\sigma^2_{\Delta\beta/\beta} + 4\frac{\sigma^2_{VTH}}{(V_{GS} - VTH)^2}} \tag{2.5}$$

Using typical values for the involved quantities, a $\sigma_{\Delta I/I}$ in the order of 1-5 % is obtained. To minimize it, large overdrive voltages should be chosen, and the area of the device should be increased.
Fig. 2.2 shows a CMOS fully-differential amplifier with resistive load. In this case, offset voltage is tied only to mismatch errors, whereas in the single-ended output amplifier the offset voltage depends mainly on errors on the nominal value of the parameters. Input offset voltage v_{io} is defined in this case as the input voltage to be applied to have $V_{out} = 0$, or:

$$I_{D1}R_1 = I_{D2}R_2 \tag{2.6}$$

and is given by:

$$v_{io} = V_{GS1} - V_{GS2} = V_{TH1} - V_{TH2} + \sqrt{\frac{2I_d1}{V_{GS1} - V_{TH1}}} - \sqrt{\frac{2I_d2}{V_{GS2} - V_{TH2}}} \tag{2.7}$$

Considering Eq. 2.6 and defining $\Delta\beta$ as the difference between β_1 and β_2 and β their average value, and ΔR and R in a similar manner, it is possible to show that:

$$v_{io} = \Delta V_{TH} + \frac{V_{GS} - V_{TH}}{2}\left(-\frac{\Delta R}{R} - \frac{\Delta\beta}{\beta}\right) \tag{2.8}$$

It should be noted that in this case the impact of ΔV_{TH} is not reduced by the biasing conditions but depends only on the area and layout of the differential pair. It is convenient to choose in this case a low overdrive voltage to decrease the effect of β and resistors mismatch.
As described above, offset is a major concern when high resolution circuits with DC capabilities have to be designed. These two examples show that also

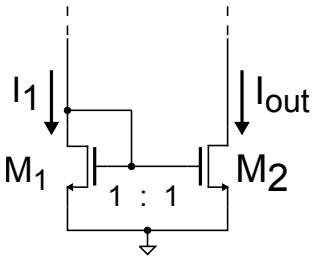

Figure 2.1: Simple current mirror with mirror coefficient equal to 1.

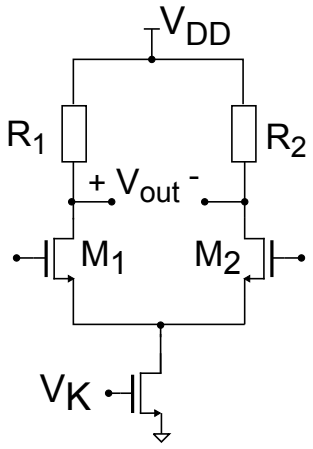

Figure 2.2: Differential amplifier with resistive load.

in simple circuits an offset in the mV range can easily arise, also using large areas and accurate layout. Besides, gate area is traded with channel capacitance, and, in turn, with speed. As an example, if a σ_{VTH} of around 1 mV is required, a gate area of around 25 µm^2 is required, resulting into a gate capacitance of 250 fF for a 180 nm process. Moreover, offset usually exhibits temperature dependence and variation with the aging of the devices. In commercial amplifiers it is often present an offset-nulling terminal, to compensate for the mismatch in various ways, but the compensation is still not robust to ageing and temperature. On the other hand, techniques like post-production laser trimming are effective but very expensive. For these reasons, dynamic offset compensation techniques have been developed and are extensively used in sensor interfacing and when very low offset level is required.

2.2 Dynamic offset compensation techniques

As extensively described above, low offset circuit are mandatory in several high accuracy applications. The purpose of dynamic offset compensation techniques is to dynamically remove from an amplifier the DC offset. These techniques are also able to significantly reduce at the same time the flicker noise level and , besides to high precision amplifiers, can be also applied to comparators, ADCs, DACs, integrator and other elementary stages of complete systems.
The most popular offset compensation techniques are Chopper Modulation, or Stabilization (CHS), Autozeroing (AZ) and Correlated Double Sensing (CDS). A distinction can be operated: while the chopper technique is basically a modulation and is performed in the continuous-time domain, autozeroing a circuits

involves sampling and noise fold-over; CDS can be represented as a particular case of autozeroing, involving two distinct sampling of offset and low frequency noise in a single phase and is used mainly is switched capacitor circuits.

2.2.1 Autozero and Correlated Double Sampling

Autozero

Fig. 2.3 represents a simplified schematic of an autozeroed amplifier. The finite gain amplifier A has an input referred noise source V_n. The latter represents thermal and flicker noise and offset contributions. During the autozero phase,

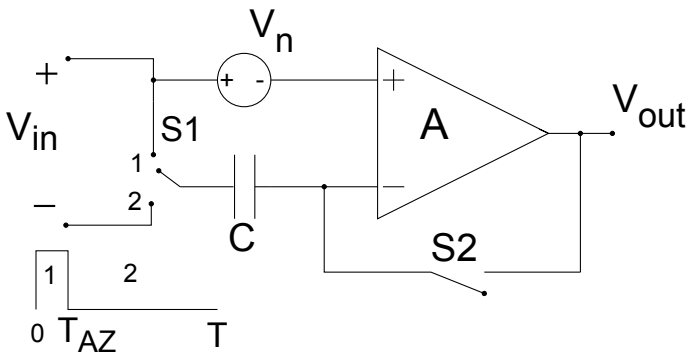

Figure 2.3: Principle of working of autozeroed amplifiers. Block A is a finite gain amplifier.

lasting from 0 to T_{AZ}, S2 is closed and S1 is connected as shown in the figure. In this phase the amplifier is closed in a unity-gain configuration and V_n is sampled on the capacitance C, thanks to the virtual short circuit. During the signal amplification phase, S2 opens and the signal gets connected to the amplifier through the capacitance C, which is still holding the sampled offset. Thus, at the output of the amplifier during the n-th signal phase we have:

$$V_{out}[n] = A\left[V_{in}(t) + V_n(nT_{AZ}) - V_n(t)\right] \tag{2.9}$$

The components of V_n that can be considered constant over a period T are then cancelled, as in the case of a DC offset, or strongly reduced, as in the case of $1/f$ noise. The main drawback of this technique is the sampling of the wide-band thermal noise: the autocorrelation between two thermal noise samples decreases very fast as the time distance increases and the AZ process results to be uneffective. On the contrary, due to undersampling, the thermal noise PSD (Power Spectral Density) folds over, resulting into an increased noise at the input. A complete analysis on the effect of AZ on noise is given in [2.3].

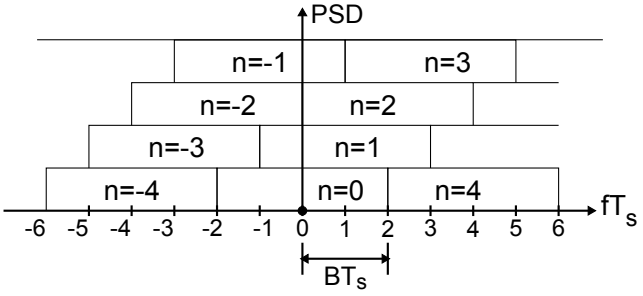

Figure 2.4: Representation of aliasing of an ideal low-pass filtered white noise, sampled at $1/T/$.

Here a brief description is reported. As stated before, a fold-over component of noise is present at the input due to sampling ($V_n(nT_{AZ})$), given by:

$$S_{fold}(f) = \sum_{n=-\inf}^{n=\inf} |H_(f)|^2 S_N\left(f - \frac{n}{T}\right) \tag{2.10}$$

where $S_N(f)$ is the noise PSD and $H(f)$ is given by:

$$|H(f)|^2 = |\mathrm{sinc}(\pi f T)|^2 \tag{2.11}$$

where T is defined as the AZ period and $\mathrm{sinc}(x)$ is equal to $\sin(x)/x$. The presence of the sinc function is due to the hold operation on C. The PSD $S_n(f)$ can be written as:

$$S_N(f) = S_0\left(1 + \frac{f_k}{|f|}\right) \tag{2.12}$$

where S_0 is the thermal noise level and f_k is the corner frequency, ranging in CMOS amplifiers from 1 to 100 kHz. To easily understand the effect of AZ on thermal noise, the latter is considered as an ideal low-pass filtered white PSD, with bandwidth B equal to the band of the amplifier. The aliasing occurring is clearly explained by Fig. 2.4, where the white noise is ideally low pass filtered with bandwidth B equal to $2/T$, where $1/T$ is the AZ period, which corresponds to the sampling frequency. The noise spectrum is shifted by the n multiples of the AZ frequency. The first replica, centered in 0, is subtracted from the non-sampled signal, $v_n(t)$ and is thus cancelled, if the effect of the $\mathrm{sinc}(\pi f T)$ can be neglected. The number N of noise replica summed in the base band is given by B/f_{AZ} where f_{AZ} is equal to $1/T$. Thus, considering positive and

negative indexes, we obtain:

$$S_{fold-white} = \sum_{n=-N, n\neq 0}^{N} S_0 \left(f - \frac{n}{T}\right) \mathrm{sinc}^2(\pi f T) = (2N-1)\, S_0 \cdot \mathrm{sinc}^2(\pi f T) \tag{2.13}$$

The undersampling factor is usually not so small. Actually, the bandwidth of the amplifier should be large enough to let the output settle into T_{AZ}, and, in turn, T_{AZ} is very smaller than T. Thus, to have good noise performances of the AZ amplifiers it is necessary to minimize S_0. This leads to an increase of the current consumption.

As long as flicker noise is concerned, a similar analysis can be performed [2.3]. However, it can be observed that if f_{AZ} is higher than f_k, no flicker noise fold-over is present in the base band and the cancellation is effective.

Typically, AZ can be applied either in open-loop or closed-loop configurations. Fig. 2.5 shows the AZ operated in the open-loop configuration, at the output of the amplifier. During AZ phase, Av_{io} is sampled on the capacitance C and

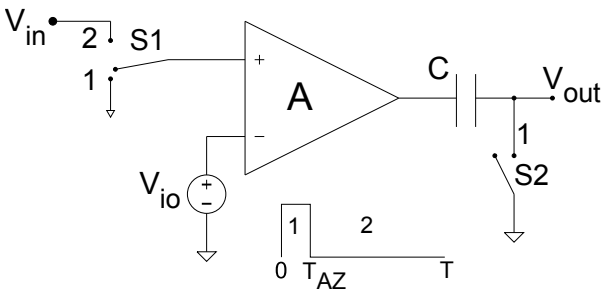

Figure 2.5: Open-loop AZ at the output of the finite gain amplifier A.

remains stored during the signal phase, being then subtracted and cancelling the offset. This technique works only if the output does not saturate and is then applicable only to finite gain amplifiers. It should be noted that an error on the sampled voltage on C at the end of AZ phase is then referred to the input divided by A. Thus, the error given by the charge injected by S2 on C is reduced. More on the charge injection topic will be given in the following.

As stated above, open-loop autozero is not suited to cancel offset of high gain amplifiers, such as operational amplifiers. In this case, closed-loop cancellation is preferred. Actually, the amplifier shown in Fig. 2.3 employs closed-loop AZ. During the offset sampling phase, the amplifier is closed in unity-gain configuration and does not saturate. In this way it is possible to amplify signals smaller than the offset level without incurring into output saturation. The main drawback of this simple configuration is the error related to charge injection.

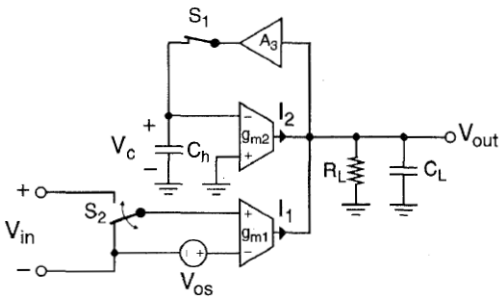

Figure 2.6: Offset compensation using an additional nulling input, after [2.3] (© [1996] IEEE).

It can be easily shown that residual offset V_{io-res} in this case is given by:

$$V_{io-res} = \frac{V_{io}}{A} + \frac{q_{inj}}{C} \tag{2.14}$$

where q_{inj} is the charge injection contribution. This problem can be mitigated using the architecture represented in Fig. 2.6 [2.3]. Here, the gain A_1 from the signal input to the output is made larger than the gain A_2 from the nulling port to the output. In this way, the error given by q_{inj} sampled on C_h is reduced by the ratio A_2/A_1. The working principle can be summarized: if the inputs are short-circuited and S1 is still open, the output V_{out} is nulled if $I_2 = -g_{m2}V_c$ is equal to $-I_1 = g_{m1}V_{os}$, i.e. if $V_c = -g_{m1}/g_{m2}V_{os}$. The ratio g_{m1}/g_{m2} should be sized to make V_c larger enough of q_{inj}/C_h, but not so large to saturate g_{m2}. The compensation voltage V_c is set during the AZ phase (S1 and S2 closed), thanks to the closed loop configuration. Defining A_1 as $g_{m1}R_L$ and A_2 as $g_{m2}R_L$, we obtain for the residual offset:

$$V_{io-res} \approx -\frac{V_{os}}{A_2 A_3} - \frac{A_2}{A_1}\frac{q_{inj}}{C_h} \tag{2.15}$$

The additional input port can be designed in several ways. A possible implementation is shown in Fig. 2.7, where M_3 and M_4 constitute the additional differential pair. By applying the appropriate voltage to their input, it is possible to compensate the offset current $I_1 - I_2 = g_m v_{io}$.

One of the major drawbacks of the circuit presented above is that the signal is not continuosly connected to the amplifier and for a small amount of time T_{AZ} the output is not valid. This can represent a problem in some applications. To overcome this issues, some architectures have been developed. Ping-pong technique [2.4] relies on the duplication of the autozeroed amplifier. In this way, when the first amplifier is autozeroed, the second is connected to the signal

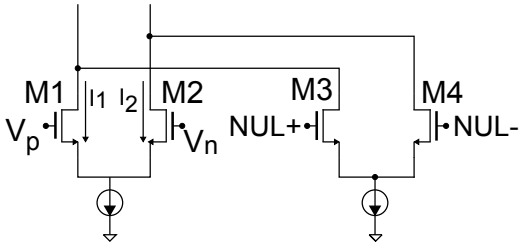

Figure 2.7: Possible realization of a nulling input differential port. M_3 and M_4 are the nulling differential pair.

and vice versa. Fig. 2.8 shows the resulting architecture, with the necessary phases. The complementary input (NMOS and PMOS) amplifiers A1 and A2

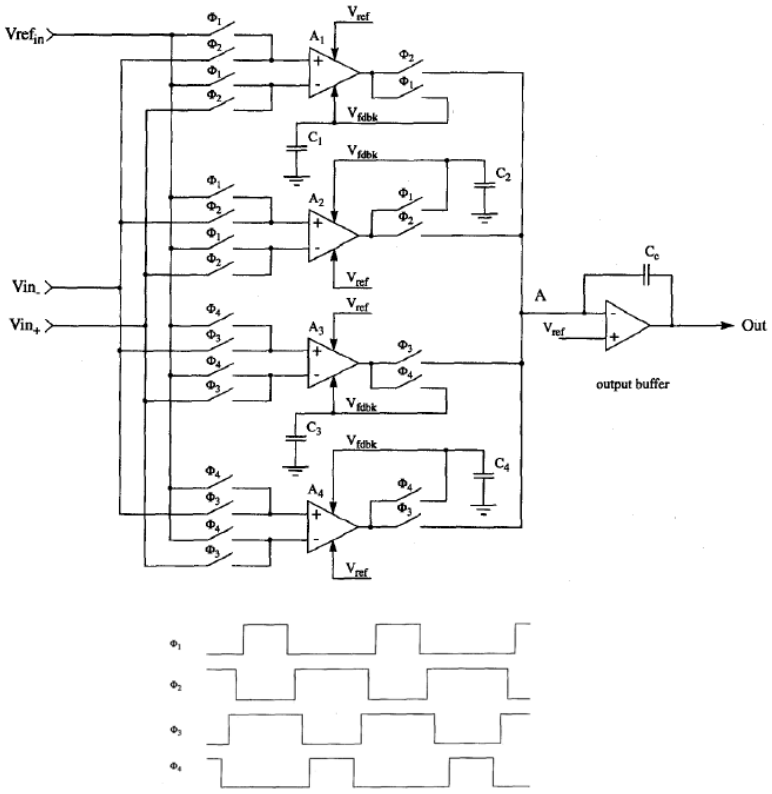

Figure 2.8: Ping-pong operational amplifier, after [2.4] (© [1996] IEEE).

are autozeroed during ϕ_1 and connected to the signal during ϕ_2. Complementary amplifiers A3 and A4 guarantee the continuous-time functionality being connected during ϕ_3 and autozeroed during ϕ_4. Main drawbacks of this configuration are the doubled power consumption and area and the presence of spikes due to the switching.

A more efficient solution is presented in [2.5]. Here, the main amplifier is never disconnected from the signal, while the autozeroed nulling amplifier generates the nulling signal necessary to compensate the offset of the main amplifier. This configuration works only if the overall amplifier is closed in negative loop in such a way that V_{io} appears across the inputs of the main amplifier and can be read by the nulling amplifier. Fig. 2.9 shows this architecture. The main

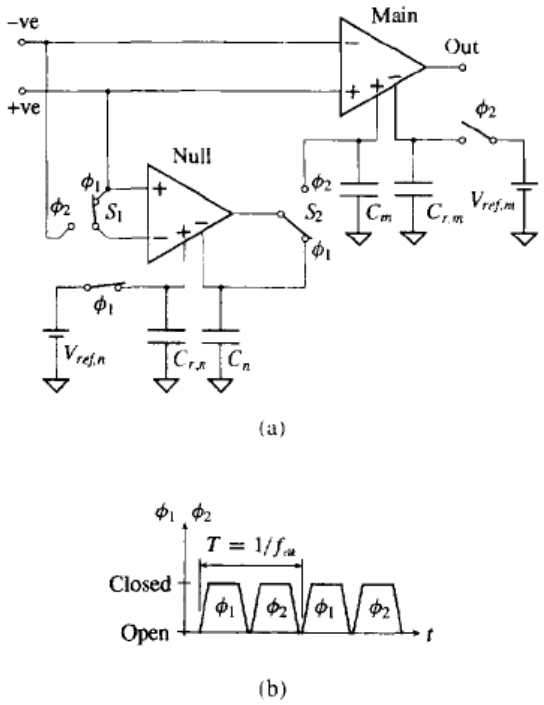

Figure 2.9: Continuous-time AZ amplifier. Architecture (a) and phases (b), after [2.5] (© [1995] IEEE).

drawback is represented by the large sampling capacitors required to minimize the error introduced by charge injection and leakage, although the former can be mitigated using a differential structure. Stability requirements include the unity-gain stability of both the amplifiers during phase ϕ_1. During phase ϕ_2 a zero appears in the frequency response [2.5] and the amplifier results to be stable only in a given gain range.

Correlated Double Sampling

A particular implementation of the Autozero technique is the Correlated Double Sampling. This technique is particularly popular in discrete time circuits,

such as Switched Capacitor. The principle of operation can be explained making reference to Fig. 2.10. A switched capacitor inverting amplifier is repre-

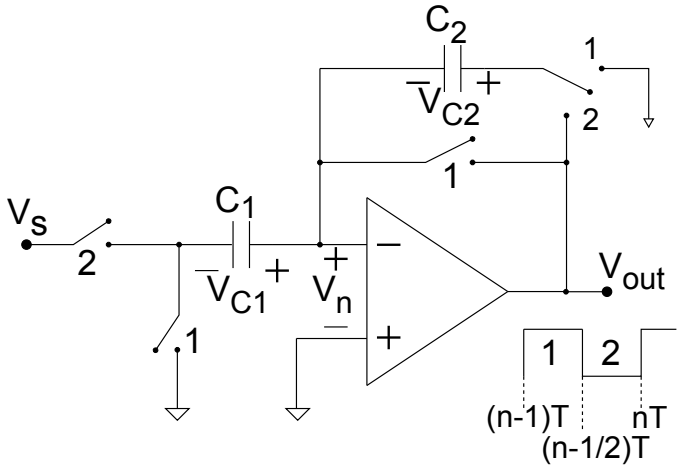

Figure 2.10: Switched capacitor inverting amplifier implementing Correlated Double Sampling to cancel offset and reduce flicker noise.

sented, with its input referred offset and noise voltage source V_n. The signal V_s is assumed to be constant over a period. At the end of phase 1, the voltages V_{C1} and V_{C2} are as follows:

$$V_{C1}^{(1)} = V_n^{(1)} \tag{2.16}$$

$$V_{C2}^{(1)} = -V_n^{(1)} \tag{2.17}$$

$$V_{out}^{(1)} = V_n^{(1)} \tag{2.18}$$

At the end of phase 2, instead:

$$V_{C1}^{(2)} = V_s - V_n^{(2)} \tag{2.19}$$

$$V_{C2}^{(2)} = V_{C2}^{(1)} + \frac{\Delta Q}{C_2} \tag{2.20}$$

$$V_{out}^{(2)} = V_n^{(2)} + V_{C2}^{(2)} \tag{2.21}$$

and:

$$\Delta Q = -C_1 \cdot V_s \tag{2.22}$$

Thus, at the end of phase 2 we have:

$$V_{out}^{(2)} = V_n^{(2)} - V_n^{(1)} - \frac{C_1}{C_2}(V_s) \tag{2.23}$$

It is clear that correlated contributes to V_n are cancelled or strongly reduced. While it is immediately clear that DC offset is cancelled over a period, it is useful to gain a deepened view on the way noise is processed. Taking into account the N-th period, as shown in figure, we can write for the noise contribution:

$$V_{out} = V_n[n] - V_n\left[n - \frac{1}{2}\right] \tag{2.24}$$

where $V_n[n]$ and $V_n\left[n-\frac{1}{2}\right]$ represent the noise contribution sampled at nT and $(n-1/2)T$, respectively. A simplified spectral analysis can be performed taking into account Fig. 2.11. Noise contribution is first delayed of half a period, then subtracted from the original signal and sampled. Then, a hold operation takes place. The noise power spectral density is processed by the following function

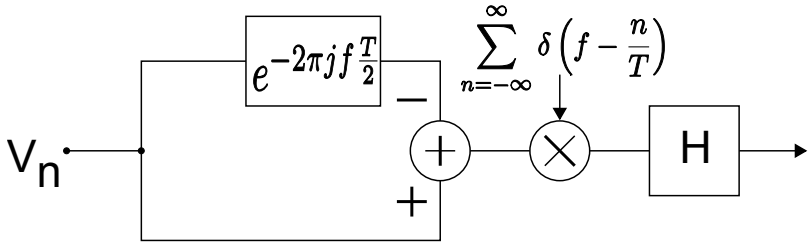

Figure 2.11: Simplified block description of noise processing in a CDS amplifier.

and then sampled:

$$|H_s(f)|^2 = 4\sin^2\left(\pi f \frac{T}{2}\right) \tag{2.25}$$

This function has a zero at DC and at even multiples of $2/T$, cancelling the offset and strongly reducing flicker noise. After this, sampling takes place. Thanks to the zeros placed by H_s, only even harmonics of thermal noise contribute to the output noise spectrum. The hold operation limits the signal energy introducing a sinc filtering. Considering positive and negative indexes and under-sampling, we have at low frequencies a total thermal noise contribution equal to $4NS_0$, where S_0 is the thermal PSD, and N is given by BT, where B is the bandwidth of the amplifier. It should be noted that the noise contribution seems to be double than in AZ amplifiers, but required bandwidth in CDS amplifier is lower than in autozeroed, if the same period T is considered. This because CDS amplifier output has to settle in $T/2$ rather than in T_{AZ}, which is considerably smaller.

Both of the techniques described above suffer of an increased thermal noise level at base band, requiring often high power consumption if an high dynamic range is required. Moreover, they suffer of errors related to charge injection

and clock feedthrough that can be only partially mitigated using a differential structure.

2.2.2 Chopper modulation

Chopper modulation [2.3] is significantly different than AZ or CDS, since it doesn't involve sampling operation, and it is rather a continuos-time technique. Basically, low frequency noise and offset are shifted at higher frequencies by modulation and rejected with a low pass operation. The architecture of a chopper amplifier is depicted in Fig. 2.12. It consists of a finite gain amplifier A with

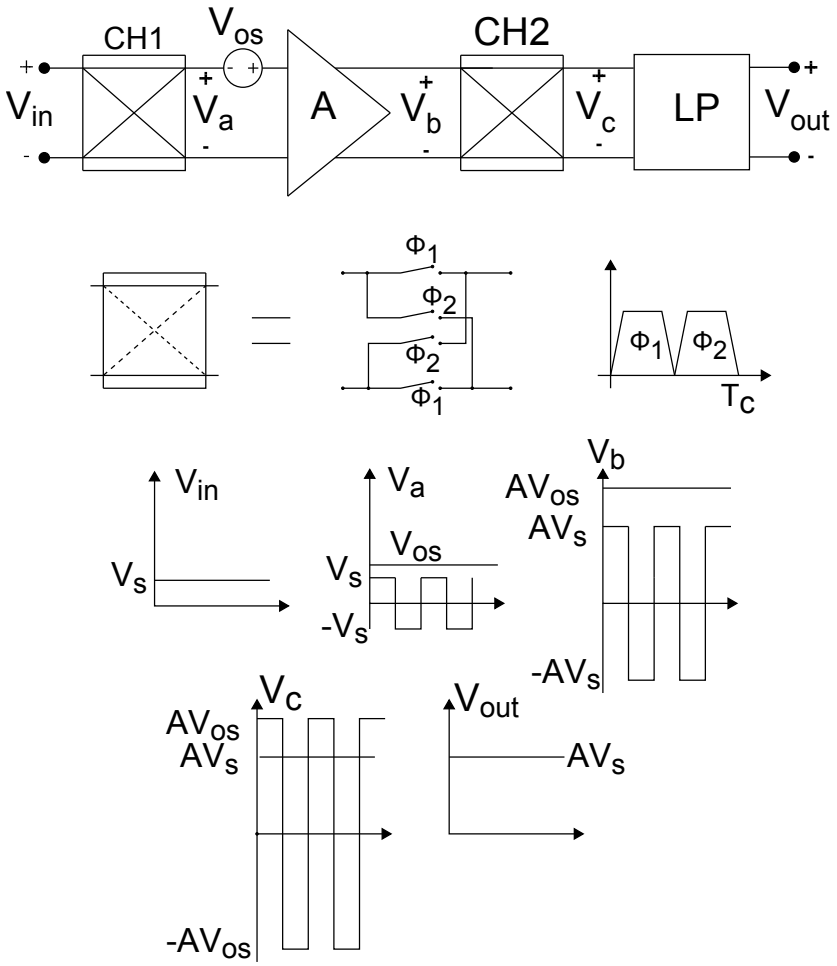

Figure 2.12: Chopper amplifier architecture with modulator structure, phases and idealised waveforms.

input referred offset V_{OS}, two frequency modulators CH1 and CH2 whose structure is shown in the figure and a low pass filter LP. The modulators are driven

by the phases ϕ_1 and ϕ_2 with frequency f_{ch} equal to $1/T_{ch}$. As represented in Fig. 2.12, which shows separately the way offset V_{os} and signal V_s are treated, signal is first modulated by CH1 and then demodulated by CH2. On the other hand offset is first amplified by A, then modulated towards high frequencies by CH2 and finally rejected by LP. Here the bandwidth of the amplifier is supposed infinite. If the amplifier has a limited bandwidth, high frequency glitches appear. This happens because V_{in} is ideally modulated, whereas the amplified signal V_b is sligthly delayed by A. The modulated offset is often referred to as offset ripple and has the same chopper frequency f_{ch}.
It is possible to describe what happens in the frequency domain making reference to Fig. 2.13. The modulators CH1 and CH2 operate the modulation by a

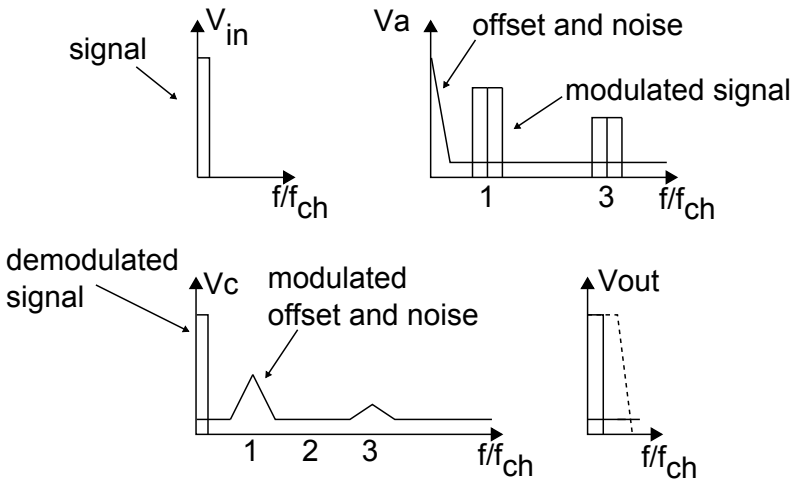

Figure 2.13: Idealised spectra of signal and input noise at the different stages of the chopper amplifier.

zero average square wave. Its Fourier coefficients are given by:

$$\begin{aligned} m_k &= 0 \text{ if } k = 0 \\ m_k &= \frac{2}{k\pi} \text{ if } k = \pm 1, \pm 5, ... \\ m_k &= -\frac{2}{k\pi} \text{ if } k = \pm 3, \pm 7, ... \end{aligned} \tag{2.26}$$

It is important to recall the Parseval's theorem:

$$\sum_{k=-\infty}^{k=+\infty} |m_k|^2 = 1 \tag{2.27}$$

Taking into account the signal V_s and supposing an infinite bandwidth amplifier, we have after CH1 and amplication:

$$V_b = A \sum_{k=-\infty}^{k=+\infty} M_k V_s \left(f - k f_{ch}\right) \tag{2.28}$$

After the demodulation operated by CH2 we have:

$$V_c = A \sum_{k=-\infty}^{k=+\infty} \sum_{h=-\infty}^{h=+\infty} M_k M_h V_s \left[f - (k+h) f_{ch}\right] \tag{2.29}$$

The LP filter selects only the harmonics translated back into base-band, for what $h = -k$ holds. Then, since $M_{-k} = M_k^*$:

$$V_{out} = A \sum_{k=-\infty}^{k=+\infty} M_k M_{-k} V_s \left(f\right) = AV(f) \sum_{k=-\infty}^{k=+\infty} \left|M_k\right|^2 = AV(f) \tag{2.30}$$

Thus, chopper modulation does not alter the signal spectrum.
On the other hand, noise and offset, represented by V_{os}, are initially amplified and then modulated by CH2. The amplifier input noise $S_N(f)$ has the form of Eq. 2.12, where f_k is the corner frequency. Then, we can write for the noise PSD after CH2:

$$S_c\left(f\right) = A^2 \sum_{k=-\infty}^{k=+\infty} \left|M_k\right|^2 S_N\left(f - k f_{ch}\right) \tag{2.31}$$

Although the noise spectrum is still formed by a summation, replicas are scaled down by $1/n^2$ and their contribution to the base-band noise decrease rapidly. Thermal and flicker noise contributions can be separately analyzed. If the amplifier has an infinite bandwidth, recalling the Parseval's theorem, it can be observed that thermal noise PSD in base-band remains unchanged. If the amplifier has a finite bandwidth B, resulting output thermal noise PSD approaches 90% of S_0 for B/f_{ch} around 6 [2.3]. The $1/f$ noise contribution can be also described: considering a bandwidth B much larger than f_{ch}, the chopped flicker noise PSD can be approximated by [2.3]:

$$S_{c-f}\left(f\right) \approx 0.8525 S_0 \frac{f_k}{f_{ch}} \tag{2.32}$$

where f_k is the amplifier corner frequency. Thus, if f_{ch} is larger than f_k, flicker noise contribution can be strongly reduced. The total noise PSD at base-band

can be finally approximated by:

$$S_c(f) \approx S_0 \left(1 + 0.8525 \frac{f_k}{f_{ch}}\right) \tag{2.33}$$

It can be observed that in chopper amplifiers, if f_{ch} is properly chosen, output noise PSD is significantly lower than in AZ and CDS amplifier, for equal amplifier PSDs. Thus, this technique offers the best trade-off among noise and power consumption. Its main drawback resides in the fact that the LP filter cut-off frequency has to be lower than f_{ch}, thus limiting the disposable amplifier bandwidth. This is not a problem in low frequency circuits, such as sensor interfaces. In case this represents a problem, more sofisticated architectures have to be implemented, like multi-path, broad-band chopper stabilized amplifiers [2.6]. Some examples of advanced chopper amplifiers will be given in the next chapter.

2.2.3 Offset ripple

As described in the previous section, the modulated offset appears at the output of the chopped amplifier as a square wave with period T_{ch} superimposed to the amplified signal. When dealing with high gain amplifiers, the amplitude of the modulated offset can be as large as to saturate the amplifier, limiting its output swing. Furthermore, it should be cancelled to extract the correct signal value without introducing sampling errors if an ADC follows the amplifier.
The traditional chopper amplifiers, represented in Fig. 2.12, relies on the low pass filtering operated by the low pass filter LP to reject offset ripple and $1/f$ noise. This technique suffers from several issues. First of all, if the amplifier gain is low, the filter offset and noise performances would adversely impact the overall amplifier performances. This can occur when the input signal amplitude reaches some tens of mV. Furthermore, to guarantee a low input referred residual DC offset, chopper frequency f_{ch} is usually chosen in the kHz range. This point will be clarified in the next section. Such a low frequency offset ripple requires a low LP filter cut-off frequency to be properly removed. Low-pass filters with kHz or sub-kHz singularities usually need a very large silicon area to be integrated, especially in case of strict noise constraint, as will be widely discussed in Chap. 6. For this reason, external filter are sometimes used [2.7].
In the literature, some techniques have been recently proposed to overcome this issue and to facilitate the complete integration of chopper amplifiers with

reasonable amount of silicon area. The advantages and issues of some of these approaches will be discussed in the next chapter. In this thesis a novel approach has been developed, consisting in merging amplifier and low pass filter in a single block. The proposed approach will be described later.

2.2.4 Modulator non-idealities and residual offset

Residual offset in differential chopper amplifiers is mainly due to charge injection and clock feedtrough mismatch taking place into the input modulator, usually realized using MOS switches. Generally speaking, any odd-simmetry spike generated in the input modulator will be amplified and demodulated by CH2. Then, the spikes will be averaged by the LP filter giving rise to an undesired DC component at the output.
The phenomena giving rise to spikes can be basically divided into charge injection and clock feedthrough, which can be explained making reference to Fig. 2.14. The figure represents an ideal sample and hold circuits, with parasitic and overlap capacitances. When the clock applied to the gate goes to 0,

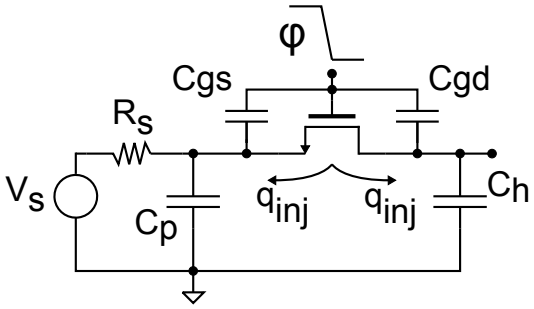

Figure 2.14: Single MOS S/H circuit.

the channel charge flows to the source and drain diffusions. The partition of these charges is not easy to define and depends on the impedance at the source and drain terminals. It is usely recognized [2.3] that the charge is equally split between source and drain if either the clock transition time is shorter than $R_{on}C$ (independent on the ratio C_p/C_h, where R_{on} is the switch on-resistance, or $C_h = C_p$. However, this phenomena is hard to accurately predict or simulate. An estimation will be given in the following. The channel charge can be written as:

$$Q_{ch} = C_{ox}WL\,(V_{GS} - V_{TH}) \tag{2.34}$$

where C_{ox} is the oxide capacitance per unit area. If the charge is equally split, the error ΔV_{D-inj} on C_h will be given by:

$$\Delta V_{D-inj} = \frac{Q_{ch}}{2C_h} = \frac{C_{ox}WL\left(V_{GS} - V_{TH}\right)}{2C_h} \tag{2.35}$$

On the other hand, clock feedthrough is due to the coupling of the clock to the output through the overlap capacitance C_{gd}. Its contribution ΔV_{D-ck} is given by:

$$\Delta V_{D-ck} = V_{ck}\frac{WC_{ov}}{WC_{ov} + C_h} \tag{2.36}$$

where C_{ov} is the overlap capacitance per unit length and V_{ck} is the clock swing. If a differential NMOS modulator is considered (Fig. 2.15), differential operation ensures a reduction of the injection charge and clock feedthrough related offset. In this case, the residual offset is determined by the mismatch of the injected charges on the amplifier input capacitances C_{in}. Each time the switch

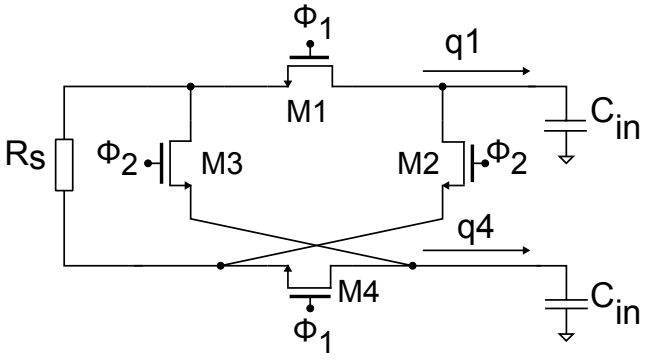

Figure 2.15: Chopper modulator.

array changes its state, a certain amount of charge q_1 and q_4, resulting from the switch mismatches, flows into C_{in}. Assuming equal splitting, the charge mismatch due to injection can be written as [2.8]:

$$\Delta q_{inj} = \frac{1}{2}WLC_{ox}\left[\left(\frac{\Delta W}{W} + \frac{\Delta L}{L}\right)\left(V_{GS} - V_{TH}\right) - \Delta V_{TH}\right] \tag{2.37}$$

where $\Delta W/W$, $\Delta L/L$ and ΔV_{TH} are the mismatches of width, length and threshold voltage of the switches, respectively. The clock feedthrough mismatch contribution is given by:

$$\Delta q_{cf} = C_{ov}V_{ck}\frac{\Delta C_{ov}}{C_{ov}} \tag{2.38}$$

where $\Delta C_{ov}/C_{ov}$ is the mismatch of the overlap capacitance. The total charge injected is then given by:

$$\Delta q_{tot} = \Delta q_{cf} + \Delta q_{inj} \tag{2.39}$$

Thus, due to the differential circuit nature and considering the worst case, the output spike will be given by:

$$V_{spike} = 2\frac{\Delta q_{tot}}{C_{in}} \tag{2.40}$$

Assuming an exponential decay, the time constant τ is given by:

$$\tau = (R_{on} + R_s)C_{in} \tag{2.41}$$

and the resulting DC offset value is given by, if the amplifier has an infinite bandwidth:

$$V_{os-out} \approx AV_{spike}2\frac{\tau}{T_{ch}} \tag{2.42}$$

Since it is more interesting to estimate the offset standard deviation, rather than its absolute value, it is necessary to consider the standard deviation of Δq_{inj} and Δq_{cf}, which can be obtained using process design parameters. As an example, considering a 0.18 µm process with 1.8 V clock swing, W equal to 1 µm , L equal to 0.18 µm, both with a 5% mismatch, $V_{GS} - V_{TH}$ equal to 0.35 V, a σ_{VTH} of 15 mV, a C_{ov} of 1 fF with a mismatch of 5% and C_{ox} equal to 10 fF/µm^2, the switch R_{on} resistance is equal to around 2 kΩ and σV_{os} results to be around 150 nV for f_{ch} equal to 50 kHz. This simplified estimate typically tends to underestimate the residual offset. It should also be noted that for minimum length transistors mismatch is typically higher than what expected and that for less scaled technology nodes the gate area increases and thus the injected charge. It can be also stated that charge injection related residual offset increases with approximately $\sqrt{W}$, since injected charge is proportional to W, while mismatch decreases with $\sqrt{W}$.
Usually, the charge injection contribution in a typical chopper amplifier can be estimated in a few µV for f_{ch} of a few kHz. An approach that can be adopted to reduce the absolute value of the charge injection is the use of dummy switches, as depicted in Fig. 2.16. When M_1 turns off, both M_d turns on, removing the charge injected by the former. This technique relies on equal charge splitting, which is hard to achieve, due to asymmetries in the switch layout and load impedances. Besides, while the common mode charge injection and, in turn,

the input bias current is reduced, the offset standard deviation is not affected, because the charge mismatch tends to increase due to increase of effective gate area. Besides the implementation of fully differential circuits or dummy

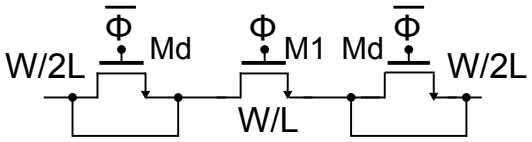

Figure 2.16: Implementation of series dummy switches.

switches, some techniques have been developed to decrease the offset introduced by the modulator non-idealities. Menolfi *et al.* [2.9] proposed a spike filtering approach. It can be observed that spikes have spectral components placed around the odd clock harmonics. Using a selective amplifier or a band-pass filter it is possible to reject their energy without degrading the signal. The authors have shown that an optimal choice for the filtering is using a 2^{nd} order band-pass filter, with the resonance frequency ω_0 matched with the chopper frequency. However, the efficiency of this technique is tightly related to the filter quality factor Q and the matching of ω_0 and f_{ch} and is very temperature-dependent. The practically achievable Q values also limit the efficiency. Another proposed solution is the nested chopper architecture [2.10]. The principle of operation is shown in Fig. 2.17. Inner modulators CH1H and CH2H are driven by a frequency f_{ch}, optimized to reduce the flicker noise. The external modulators CH1L and CH2L modulates the spikes produced by CH1H and CH2H. Their driving frequency f_{cl} has to be chosen significantly lower than f_{ch}. In this way, residual offset is reduced without altering noise performances. The LP filter should have a cut-off frequency lower than f_{ch}. The reduced available bandwidth can still be enough in some applications, like temperature sensors [2.11].

2.3 Conclusions

In this chapter, two different dynamic offset cancellation techniques have been discussed: Autozeroing and chopper modulation. While the former cancels

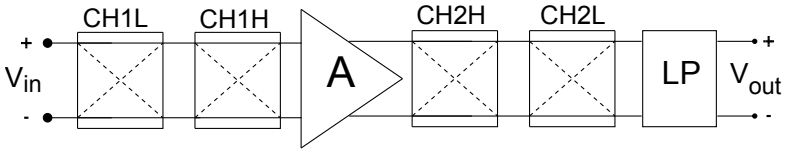

Figure 2.17: Principle of operation of nested chopper technique.

offset in the time-domain, relying on sampling, the latter employs modulation to reject offset in the frequency domain. Noise performances have been discussed. Generally, AZ or CDS amplifiers can provide a larger bandwidth with simpler implementations, at the cost of an increased noise level with respect to chopper amplifiers, due to noise undersampling.
The sources of residual offset in dynamically offset compensated amplifiers have been presented and some techniques to reduce their impact have been discussed.

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Chapter 3

Low-noise, low-offset instrumentation amplifiers

The peculiar characteristics of the instrumentation amplifiers, such as high and precise differential gain, high input resistance, high CMRR, make them ideal blocks for interfacing a wide variety of sensors. Instrumentation amplifiers are particularly suited to read MEMS flow sensors, which are characterized by small amplitude output voltage and high series resistance. Input offset and noise in the µV level are required, in order not to degrade the sensor dynamic range. To achieve these performances, dynamic offset compensation techniques have to be exploited. In this chapter, high accuracy instrumentation amplifiers proposed in the literature will be discussed.

3.1 Instrumentation amplifier characteristics

Instrumentation amplifiers are circuits capable to amplify with an accurate gain a differential signal without loading the source and rejecting input common mode voltages and are a basic building block of biomedical systems as well as of sensor reading interfaces.
Fig. 3.1 shows a reading circuit of a generic sensor represented as a differential voltage source with a common mode and a series resistance. The amplifier has a differential gain A_d, V_d is the sensor differential output and V_{CM} the sensor common mode and R_{s1} and R_{s2} are the sensor series resistances. For a balanced source we have $R_{s1} = R_{s2}$. The amplifier has a single ended output. This is a typical case in discrete systems. In integrated circuits the fully dif-

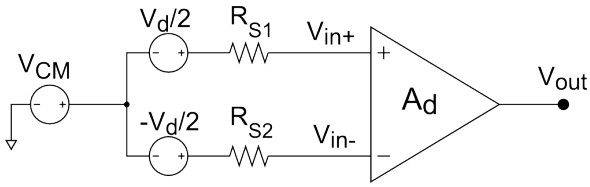

Figure 3.1: Instrumentation amplifier interfacing a sensor with differential output and series resistance.

ferential output is often preferred, in order to reject disturbances common to both terminals. Differential and common mode amplifications are given by:

$$A_d = \frac{V_{out}}{V_{id}}; \qquad A_c = \frac{V_{out}}{V_{ic}} \tag{3.1}$$

where V_{id} and V_{ic} are defined as:

$$V_{id} = V_{in+} - V_{in-}; \qquad V_{ic} = \frac{V_{in+} + V_{in-}}{2} \tag{3.2}$$

Typical features of a good quality instrumentation amplifier are:

- Accurate differential gain
- High DC and AC CMRR
- Low offset voltage and currents
- High and matched inverting and non inverting terminals input impedance
- Low noise
- Low distortion

The accurate gain is necessary for a proper sensor reading. Typical instrumentation amplifiers gain errors are lower than 1%. Usually, gain in instrumentation amplifier is obtained by means of ratios of homogenous quantities, such as resistors. In this way, temperature and process variations are compensated, at least at the first order. In addition, components of the same kind exhibit matching, which can be improved with well-known design and layout techniques, reducing the gain spread.
The CMRR quantifies the capability of the amplifier of rejecting common mode signals and is defined as:

$$CMRR = 20 \log \frac{A_d}{A_c} \tag{3.3}$$

In several applications, such as sensing the high side current from a supply, the instrumentation amplifier should be able to amplify signals in the mV range with common mode voltages variations in the order of hundred of mV. The CMRR can be divided into the DC CMRR, measuring the common-mode rejection ratio for DC signals, and into the AC CMRR, which takes into account the CMRR frequency dependence.
The input offset of an instrumentation amplifier can be modelled as shown in Fig. 3.2. The voltage offset referred to the input is represented by the volt-

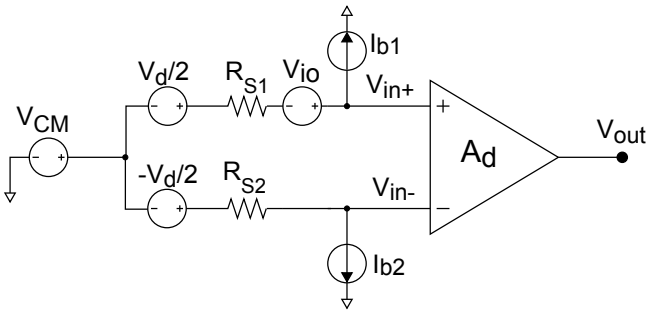

Figure 3.2: Instrumentation amplifier with input offset sources.

age source V_{io}, while I_{b1} and I_{b2} current sources represent the input currents. Defining the bias current I_b and the offset current I_{io} as:

$$I_b = \frac{I_{b1} + I_{b2}}{2}; \qquad I_{io} = I_{b1} - I_{b2} \tag{3.4}$$

and $R_{s1} = \overline{R_s} + \Delta R_s/2$ and $R_{s2} = \overline{R_s} - \Delta R_s/2$, where $\overline{R_s}$ is the average value of the source resistances and ΔR their difference, it can be obtained for the total input offset V_{IO}:

$$V_{IO} = V_{io} - \overline{R_s} I_{io} - \overline{R_s} I_b \frac{\Delta R_s}{\overline{R_s}} \tag{3.5}$$

It should be observed that input current contribution is particularly detrimental in case of high sensor resistance, as in case of MEMS thermal sensors.
An high differential input impedance is necessary to avoid loading the source. Taking into account Fig. 3.3, where input impedances R_{i1} and R_{i2} have been put into evidence, we obtain:

$$\frac{V_{out}}{V_d} = A_d \frac{R_{i1} + R_{i2}}{R_{s1} + R_{s2} + R_{i1} + R_{i2}} \tag{3.6}$$

The finite input impedance leads to a gain attenuation due to the source loading. On the other hand, if input impedance are unbalanced, a spurious differ-

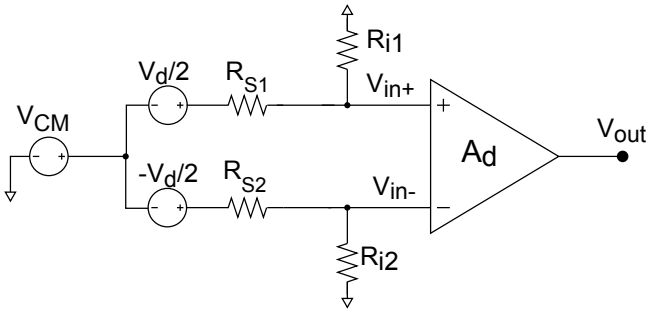

Figure 3.3: Instrumentation amplifiers with input resistances.

ential signal due to the common mode signal appears at the amplifier input. Actually, if $V_d = 0$, we have:

$$V_{out} = V_{CM}\left(\frac{R_{in1}}{R_{in1}+R_{s1}} - \frac{R_{in2}}{R_{in2}+R_{s2}}\right) \tag{3.7}$$

Defining R_{in1} and R_{in2} as $\overline{R_{in}} + \Delta R_{in}/2$ and $\overline{R_{in}} - \Delta R_{in}/2$, assuming that $\Delta R_{in} << \overline{R_{in}}$, it is possible to obtain with simple calculations:

$$V'_{IO} \approx V_{CM}\frac{\overline{R_s}}{\overline{R_{in}}}\left(\frac{\Delta R_s}{\overline{R_s}} - \frac{\Delta R_{in}}{\overline{R_{in}}}\right) \tag{3.8}$$

where V'_{IO} is the spurious differential voltage appearing at the amplifier input, which can be treated as an additional input offset. This contribution becomes more important as the ratio $\overline{R_s}/\overline{R_{in}}$ increases. The standard deviation of the input offset, considering also this contribution, can then be written:

$$\sigma^2_{V_{IO}} = \sigma^2_{V_{io}} + V^2_{CM}\frac{\overline{R_s}^2}{\overline{R_{in}}^2}\sigma^2_{\Delta R_{in}/\overline{R_{in}}} + \left(I_b\overline{R_s} + V_{CM}\frac{\overline{R_s}}{\overline{R_{in}}}\right)\sigma^2_{\Delta R_s/\overline{R_s}} \tag{3.9}$$

Besides offset, another factor that limit amplifier resolution is the input noise. Fig. 3.4 shows the input noise voltage and current sources, together with the noise sources associated with the thermal noise of the sensor resistances, V_{nR1} and V_{nR2}. The amplifier noise contribution should be made negligible with respect to the sensor noise, in order not to degrade the dynamic range of the latter. The noise at the input is then given by:

$$v_{in} = v_{nR1} + v_{nR2} + v_n - I_{n1}R_{s1} + I_{n2}R_{s2} \tag{3.10}$$

Taking into account the power spectral densities (PSD):

$$S_{in} = S_n + 2S_{n-i}R_s^2 + 2S_{nR} \tag{3.11}$$

where the PSD of the noise current sources has been considered equal, as well as that of $R_{s1,2}$. Typically, in a CMOS amplifier the input current is not relevant and its noise contribution can be neglected. The input noise PSD of a CMOS amplifier can be written as:

$$S_n(f) = S_0 \left(1 + \frac{f_k}{|f|}\right) \tag{3.12}$$

where S_0 is the thermal PSD and f_k is the corner frequency. Integrating the noise PSD over a band of interest $B = f_H - f_L$, the *rms* noise voltage is obtained:

$$v_{n-rms} = \sqrt{\int_{f_L}^{f_H} S_n(f)\mathrm{d}f} \tag{3.13}$$

Considering a crest factor of 2, the peak-to-peak noise v_{n-pp} is given by $4v_{n-rms}$. Taking into account also the source resistance noise, the total *rms* noise at the input will be given by:

$$v_{in-rms} = \sqrt{v_{n-rms}^2 + v_{R-rms}^2} \tag{3.14}$$

where v_{R-rms} is given by:

$$v_{R-rms} = \sqrt{8kTRB} \tag{3.15}$$

If $v_{n-rms} = v_{R-rms}$, the total input *rms* noise increases of a factor $\sqrt{2}$.

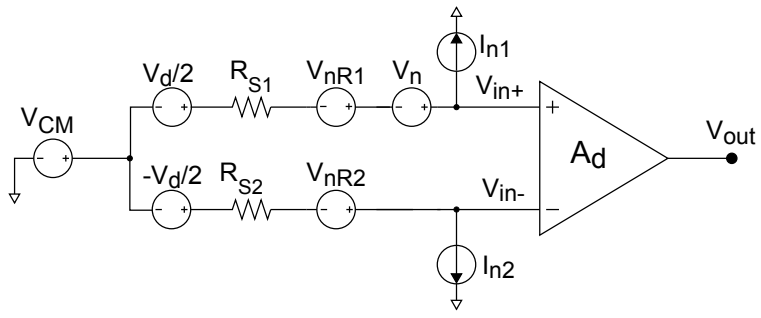

Figure 3.4: Instrumentation amplifier with noise sources.

3.2 Instrumentation amplifier topologies

The most used topology is the 3 operational amplifier (3-op-amp) instrumentation amplifier. A valid alternative is represented by the Current Feedback Instrumentation Amplifier (CFIA). In the following these structure will be presented.

3.2.1 3-op-amp instrumentation amplifier

The architecture of a differential output 3-op-amp instrumentation amplifier is depicted in Fig. 3.5. If $R_2/R_1 = R_4/R_3$, the gain G is given by:

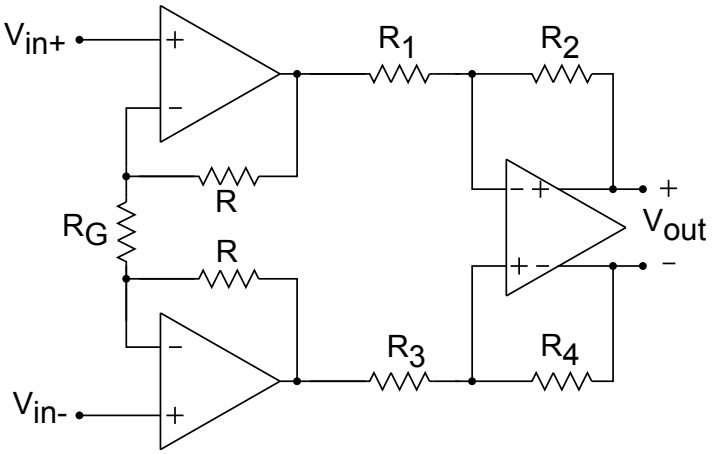

Figure 3.5: Architecture of a 3-op-amp differential output instrumentation amplifier.

$$G = \frac{V_{out}}{V_{in}} = \frac{R_2}{R_1}\left(1 + 2\frac{R}{R_G}\right) \tag{3.16}$$

In this topology, the first stage does not reject the signal common mode. The output voltage V_{out} when a common mode V_C is applied, with no hypothesis on the resistors, can be calculated:

$$V_{out} = \frac{2\left(V_{CO} - V_C\right)\left(R_2R_3 - R_1R_4\right)}{2R_1R_3 + R_2R_3 + R_1R_4} \tag{3.17}$$

where V_{CO} is the output common mode value, fixed by the internal common mode feedback. It is clear that the following condition should hold to cancel the common mode gain:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} \tag{3.18}$$

The CMRR of this instrumentation amplifier is then fixed by the matching of the feedback resistors of the second stage. This leads to poor CMRR values, in the order of 60-80 dB [3.1]. Another limitation is represented by the input range, which cannot approach the supply rails, since the operational amplifiers need to provide an output common mode voltage at the input common-mode voltage level.
Another important aspect to take into account is the noise power spectral density. Due to the presence of two operational amplifiers in the input stage with resistive feedback, an high Noise Efficiency Factor (NEF) [3.2], defined in the following equation, can be expected:

$$NEF = v_{n-rms}\sqrt{\frac{2I_{tot}}{\pi V_T 4kTB}} \tag{3.19}$$

where v_{n-rms} is the *rms* input noise voltage of the amplifier, I_{tot} the total supply current and $V_T = 26$ mV. Typical NEF values for low-power low-noise instrumentation amplifier are around 10 or lower. Another figure of merit is also used:

$$F = S_n^2 \cdot I_s \quad [\text{nV}^2 \cdot \text{mA}] \tag{3.20}$$

where S_n is the input referred noise PSD measured in nV/sqrtHz and I_s is the supply current [3.3]. The high performance instrumentation amplifier proposed in [3.1] draws a current of 2.1 mA and its noise PSD S_n is equal to 20 nV/sqrtHz and its figure of merit F results to be equal to 840. Another example is represented by the commercial FET input instrumentation amplifier INA110 (Texas Instruments). The latter has an input PSD of 10 nV/sqrtHz and a supply current equal to 3 mA, so F results to be 300. Better noise performances are achieved by the nested-chopper instrumentation amplifier, based on a 3-op-amp architecture, described in [3.4]. This amplifier has a figure of merit F equal to around 150.

3.2.2 Current Feedback Instrumentation Amplifiers

A significant alternative is represented by Current-Feedback instrumentation amplifiers (CFIA) [3.5]. They are particularly attractive since they are able to sense differential input voltages in a common mode range extended to the supply rails with a very high CMRR. Morevoer, they offer a better trade-off between noise and power consumption.
Fig. 3.6 shows the architecture of a current-feedback instrumentation amplifier.

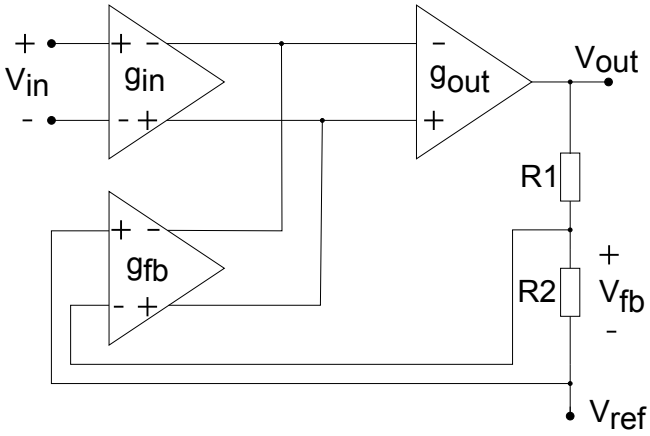

Figure 3.6: Architecture of a single-ended current feedback instrumentation amplifier.

The differential input voltage V_{in} is converted into a current by the input transconductor g_{in}. On the other hand, the transconductor g_{fb} converts into a current V_{fb}, obtained by dividing the output voltage V_{out} with the resistive divider made by R_1 and R_2. The operational amplifier g_{out} drives the output to a voltage such as the output current of g_{in} and g_{fb} cancel out. As a result, if the loop gain is high enough, indicating with g_{m1} and g_{m2} the transconductances of g_{in} and g_{fb}, respectively, and assuming that $g_{m1} = g_{m2} = g_m$, we obtain $V_{in} = V_{fb}$ and:

$$V_{out} = V_{ref} + \frac{R_1 + R_2}{R_2} V_{in} \tag{3.21}$$

Thanks to the common-mode isolation provided by g_{in} and to the transconductor output impedance balancing the CMRR of such a CFIA can reach very high values, well over 120 dB [3.6, 3.7]. In addition, as stated before, CFIAs can sense input levels at or slightly below the supply rails, thanks to the level-shifting operated by the input transistors of the transconductors. The input stage is made by simple transconductors instead of operational amplifiers. In addition, no resistors are present in the first stage. For these reasons, we can expect to achieve better noise-power tradeoffs than in the 3-op-amp case.
Possible drawbacks of this architecture are represented by the limited accuracy and non-linearity. In CMOS implementations, input transconductors will suffer from mismatch. Then, the hypothesis $g_{m1} = g_{m2}$ has to be removed and we obtain:

$$g_{m1} v_{in} - g_{m2} v_{fb} = g_{m1} v_{in} - g_{m2} \beta v_{out} = 0 \tag{3.22}$$

and:

$$A_d = \frac{g_{m1}}{g_{m2}} \frac{1}{\beta} \tag{3.23}$$

where A_d is the amplifier DC gain and:

$$\beta = \frac{R_2}{R_1 + R_2} \tag{3.24}$$

It can be observed that either a mismatch of the input transcoductances g_{m1} and g_{m2} or of the resistive feedback network leads to a gain error. Thus, due to the unavoidable mismatches introduced by the process, typical gain accuracy obtained from this architecture ranges from 1% [3.8], down to 0.1% [3.7], if particular care is taken and trimming is adopted.
Input range of the CFIA is limited: the input stages have to handle a finite voltage, but typically CMOS differential pair can handle voltages not higher than a few hundred of mV before saturating. The input range can then be improved using techniques like source degeneration. The limited input range of CMOS differential pairs also limits CFIAs linearity: a significant harmonic distortion of the transconductor output current can be expected if the input voltage is higher than a few tens of mV. However, thanks to the negative feedback, $V_{fb} = V_{in}$ and, as a consequence, the harmonics introduced by the transconductor will be strongly reduced (virtually cancelled) at the summing nodes. Nonlinearities introduced by the second stage are strongly reduced by the gain of the first stage. However, in a practical CMOS implementation the mismatch between g_{in} and g_{fb} limits the cancellation efficiency. As a result, a Total Harmonic Distortion (THD) in the order of 60-70 dB is tipically expected [3.8] from CFIAs.
Finally, another factor that limits the accuracy of CFIAs is the possible mismatch between input and output common mode (CM) voltages. Since the transconductance of a differential pair also depends on the CM voltage, even if to a second order, an additional mismatch between g_{m1} and g_{m2} is introduced, resulting into another source of gain error. When dealing with high accuracy instrumentation amplifiers, these issues have to be taken into account and solved. However, thanks to their good trade-off between noise and power consumption, their high CMRR and their extended voltage swing, CFIAs are a valid alternative to 3-op-amp instrumentation amplifiers when a sensor interface has to be designed and become preferable once the described issues have been addressed. For this reason, in the following section, low-offset current feedback instrumentation amplifiers will be described, together with high accuracy implementations described in the literature.

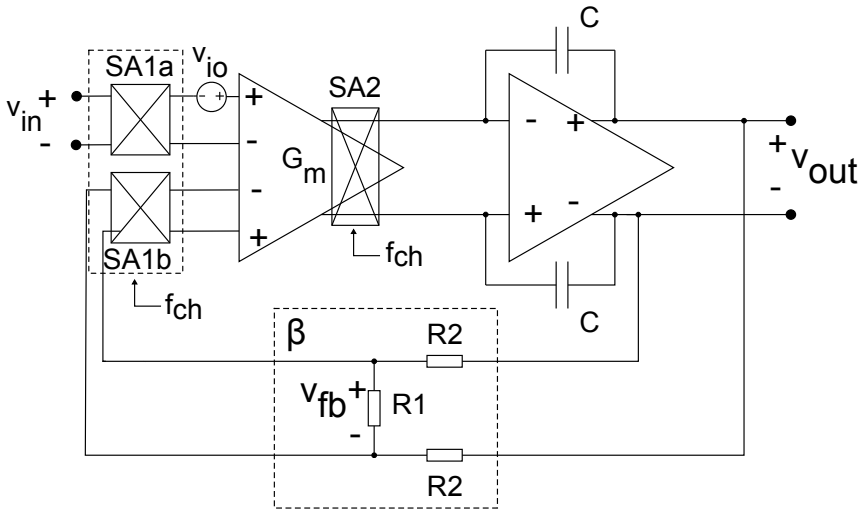

Figure 3.7: HEXAGON architecture.

3.3 Low offset current feedback instrumentation amplifiers

3.3.1 Chopper-modulated current feedback instrumentation amplifiers

In order to achieve µV resolution in a CFIA, it is necessary to compensate for the input offset and to remove $1/f$ noise from the base-band. Trimming [3.7] can be used to cancel the offset difference between the transconductors of a CFIA, using an additional adjustable transconductor. However, this technique is not effective on flicker noise, does not compensate for offset drift and is not able to reach the µV accuracy level.

Therefore, dynamic offset compensation (DOC) techniques are necessary to meet these requirements. As widely described in Chap. 2, chopper modulation offers the best trade-off between noise and power consumption and can be successfully used to build an high accuracy CFIA.

Fig. 3.7 shows a Miller-compensated differential output chopper modulated current-feedback instrumentation amplifier. It should be noted that g_{in} and g_{fb} are embedded into the double input port transconductor G_m. The feedback factor β is given by:

$$\beta = \frac{R_1}{R_1 + 2R_2} \tag{3.25}$$

The Miller's capacitors implement a pole-splitting frequency compensation. The Gain-Bandwidth product (GBW) is given by:

$$GBW = \frac{g_m}{2\pi C} \tag{3.26}$$

The closed-loop dominant pole frequency f_p is located in:

$$f_p = \beta \frac{g_m}{2\pi C} \tag{3.27}$$

Fig. 3.7 shows also the chopper modulation applied to the amplifier. Switch arrays SA1a and SA1b, operating at frequency f_{ch}, modulate the signal, shifting its spectrum around f_{ch} and its harmonics. Modulator SA2 demodulates the up-converted input signal and modulates G_m offset and flicker noise, shifting it at higher frequencies.
As described in Chap. 2, an offset ripple appears at the output due to the chopper modulation. This undesired high frequency signal added to the base-band signal should be removed to extract the signal component and to guarantee correct operation. When dealing with the CFIA represented in Fig. 3.7, modulated offset is processed by the transfer function of the amplifier:

$$H(f) = \frac{A_d}{1 + j\frac{f}{f_p}} \tag{3.28}$$

This can be intuitively explained considering that having a chopped offset current at the output of the transconductor is equivalent to have a square offset voltage at the input of the transconductor itself, but without the output modulator. This is valid until G_m is considered to have a transconductance constant over frequency. It is important then to consider the relationship between f_{ch} and the closed loop amplifier bandwidth:

- if $f_{ch} < f_p$ where f_p is the closed loop dominant pole, offset ripple is amplified by A_d and settles with a first order transient with time constant $1/(2\pi f_p)$. The peak-to-peak amplitude of the output ripple is then equal to $2A_d v_{io}$.

- the amplifier acts as an integrator for frequencies above f_p, where transfer function slope is -20 dB/dec. Thus, if $f_{ch} > f_p$, the offset square wave at the amplifier input is approximately integrated with an integrating constant g_m/C and a triangular ripple appears at the output. The amplitude

of this ripple depends on f_{ch} and can be estimated as:

$$v_{p-p} = \frac{v_{io} g_m}{2 C f_{ch}} \tag{3.29}$$

These considerations suggest a possible approach to reduce the offset ripple amplitude: increasing C in order to put f_p well under f_{ch}. This solution rapidly increases the area occupation. As an example, if $g_m = 100$ $^{-}$S and the desired $f_p = 10$ kHz, then C should be equal to about 16 pF, if A_d of 100 is considered. This value can easily increase when noise specification are taken into account and higher transonductances are required or when a lower bandwidth is required, as in the case of thermal sensors, where the bandwidth is extended no more than up to a few hundred of Hz. In addition, with this values, the offset ripple amplitude is still not negligible, since v_{p-p} would result approximately 625 mV if $v_{io} = 10$ mV an $f_{ch} = 50$ kHz. In the case of $f_{ch} < f_p$, offset ripple peak-to-peak amplitude would result as high as 2 V.
The traditional solution is to introduce a low pass filter after the chopper amplifier. However, given the finite amplifier gain, the filter offset and noise performances would adversely impact the overall amplifier performances and silicon area, especially when cut-off frequencies in the order of a few hundred Hz are required. In the following some interesting solution proposed in the literature to remove ripple from chopper operational amplifier and instrumentation amplifier will be briefly reviewed.

3.3.2 Ripple reduction techniques

Sampling approaches

A possible solution, proposed in [3.9], involves the use of a sample-and-hold filter to reduce the offset ripple in an operational amplifier. The proposed architecture is shown in Fig. 3.8, which represents a two-stage chopper operational amplifier, with a cascaded sample-and-hold. The sample-and-hold is driven at half the chopper frequency. In this way, the transfer function of this block is zero at f_{ch} and at its harmonics and the ripple is rejected without limiting the bandwidth. The filter can be put inside or outside the feedback loop. In the second case, it will introduce an additional offset. In the first case, represented in the figure, an additional pole will originate at 0.5 f_{ch} [3.9]. This partially complicates the frequency stabilization. Actually, the operational amplifier results to be conditionally stable ($A > 10$, where A is the closed-loop feedback).

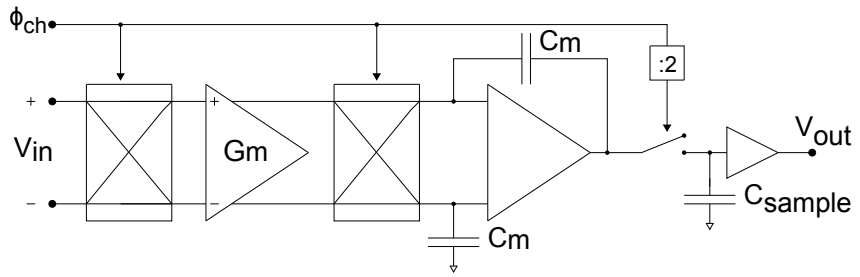

Figure 3.8: Chopper operational amplifier with sample-and-hold for ripple filtering.

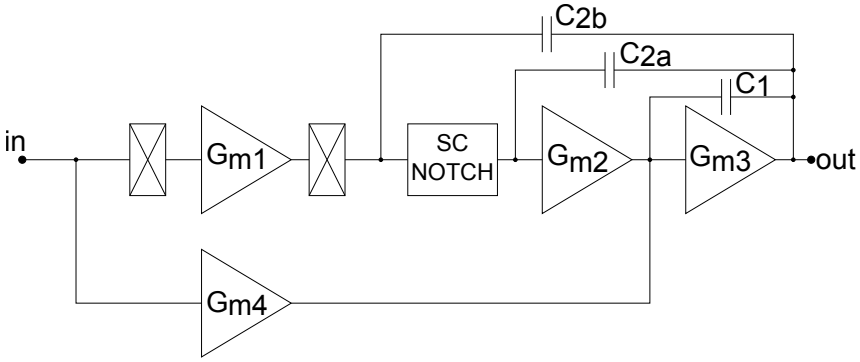

Figure 3.9: Architecture of the operational amplifier proposed in [3.3].

Due to sampling, the input noise level is relatively high (100 nV/$\sqrt{\text{Hz}}$), although a very large bias current is used (25 mA).

A more interesting ripple-reduction technique still based on sampling has been proposed in [3.3], where a chopper-stabilized opamp using a switched-capacitor (SC) notch filter with synchronous integration inside the signal path to reduce offset ripple has been presented. The amplifier topology is shown in Fig. 3.9. The amplifier is a three stage multipath nested-Miller compensated operational amplifier [3.8]. This topology consists in an high gain three stage amplifier, made of g_{m1}, g_{m2} and g_{m3} in parallel with a wider bandwidth lower gain two stage amplifier, made of g_{m4} and g_{m3}. The DC and low frequency performances are determined by the low frequency path (LFP), while the high frequency performances such as phase margin are determined by the high frequency path (HFP). By accurate design of the compensating capacitances and transconductances it is possible to match the frequency responses of both the paths in order to obtain a first-order roll-off, as in case of a traditional two-stage Miller compensated operational amplifier.

This topology can be succesfully used to design low offset, wide-band amplifiers: the offset of the wide-band amplifier is read and compensated by the low frequency path, in a very similar manner to that shown in Fig. 2.9. This

technique is often referred to as offset stabilization [3.10]. When the operational amplifier is closed in negative feedback, the LFP measures the offset at the input of G_{m4} and compensate for it. The low-frequency error of g_{m4} and g_{m2} is then divided by the DC gain of g_{m1}. However, offset and $1/f$ noise of g_{m1} still needs to be compensated. This is achieved in this work by means of chopper modulation applied to this block. As widely discussed, chopper modulation originates a large offset ripple. Here, the authors implemented a synchronous switched capacitor notch filter to reject modulated offset. The detailed implementation is shown in [3.3]. The SC notch filter introduced a delay in the signal path, requiring the modified compensation scheme shown in Fig. 3.9. Very tight specification on chopper phases are also required for proper functioning: a skew smaller than 1 ns should be achieved to correctly cancel offset ripple. Moreover, a certain noise penalty can be expected due to sampling occurring into the SC filter. However, good performances for the described operational amplifier are reported. This technique could be adopted also to cancel offset ripple into a chopper instrumentation amplifier, but would require several topology modifications and is therefore not completely suitable for it, at least in the case of CFIA.

AC-coupled ripple reduction loop

An effective continuos-time approach has been described in [3.11]. Here, the authors implemented an AC-coupled ripple reduction loop to reject the offset ripple of a current-feedback instrumentation amplifier. Output ripple is synchronously demodulated and driven to zero by cancelling the input offset. Since no sampling is involved, very good performances in terms of noise and power consumption are achieved. Fig. 3.10 shows a two-stage CFIA with the cited ripple reduction loop (RRL). Output AC offset ripple is differentiated and converted into a current by C_3, and shifted to DC by CH3. This current is then integrated by the integrator built around G_{m3}. The voltage V_o is then converted by G_{m4} into a current and fed back to the summing node. This current compensates for the offset of the input transconductors.
The synchronous demodulator formed by CH3 and the integrator acts as a narrowband filter around the chopping frequency. While the RRL has little effect at frequencies near DC, at frequencies close to the chopping frequency, however, the AC current coupled by C_3 into the synchronous demodulator will be demodulated to DC and fed back to the outputs of G_{m1}. The result is a notch

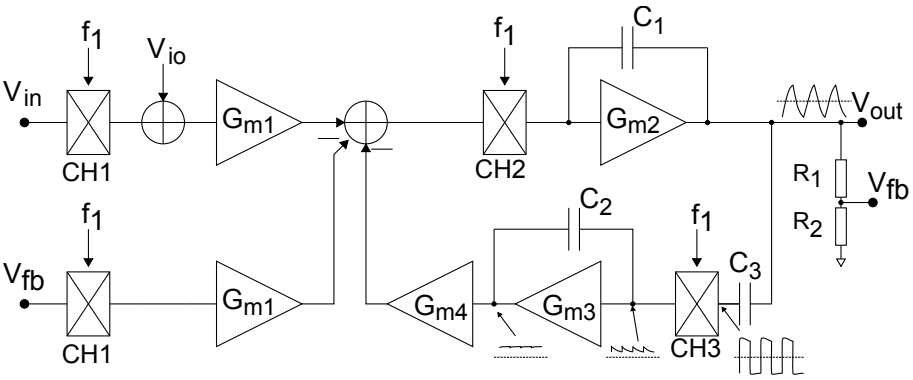

Figure 3.10: Simplified block diagram of 2-stage CFIA with the RRL.

in the amplifier forward gain at frequencies around the chopping frequency. The width of the notch is determined by the unity-gain bandwidth of the loop gain in the RRL. A detailed analysis of the loop transfer function and notch width is shown in the paper [3.11].

The proposed technique has been used to design a three-stage CFIA with a very low noise corner frequency (1 mHz), good noise performances (15.1 nV/$\sqrt{\text{Hz}}$, NEF=8.8). The GBW (gain-bandwidth) is 800 kHz, while the chopper frequency has been chosen equal to 40 kHz, in order to allow a low offset to be achieved (5 µV). Due to the presence of the RRL, a notch is also originated into the frequency response of the amplifier around 40 kHz. The result is an available bandwidth limitation. This is not a problem if the bandwidth of closed-loop amplifier is lower than f_{ch}. Additional difficulties arise when wide range of output load or closed-loop gain have to be considered, since loop gain could be influenced by the load.

Multi-path CFIA with ripple-reduction loop

The problem presented by the notch into the frequency response can be solved using a multipath topology, which enables the design of large bandwidth amplifiers. A three-stage multi-path CFIA is proposed in [3.12]. The architecture is shown in Fig. 3.11. The proposed CFIA has a low frequency path (LFP) and a high frequency path (HFP). The LFP consists in a four-stage CFIA and determines the low-frequency performances, while the HFP is a two-stage CFIA and determines the gain at high frequencies. LFP employs chopper modulation to compensate for the offset and the ripple reduction loop described above. HFP

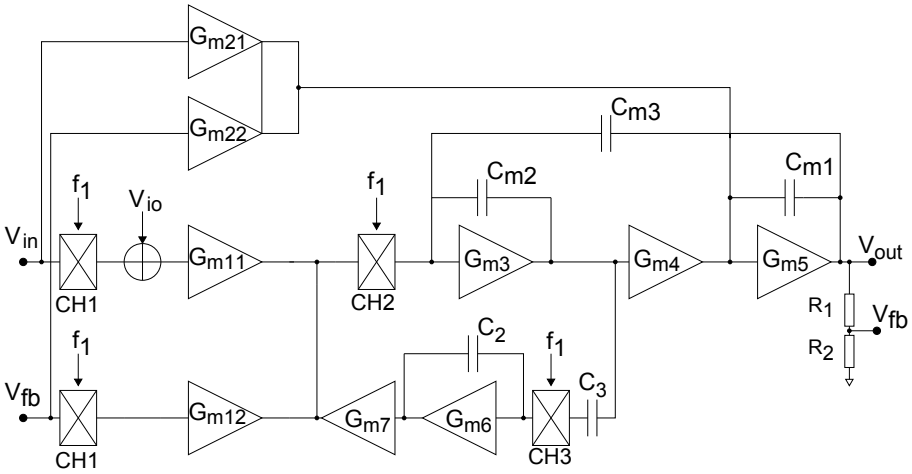

Figure 3.11: Architecture of the multipath CFIA proposed in [3.12].

offset is stabilized by the LFP. The residual offset can be written as:

$$V_{os} \approx \frac{A_{HFP}}{A_{LFP}} V_{os22} \tag{3.30}$$

At high frequencies, the HFP starts to dominate when its gain becomes higher than the gain of the LFP. The frequency at which the gains of the paths are equal is called the cross-over frequency. The cross-over frequency should be lower than f_{ch}, in order to let the HFP to bypass the notch due to the ripple reduction loop used in the LFP. The signal paths are merged with the multi-path hybrid-nested Miller compensation scheme, which helps also to obtain a smooth response [3.8, 3.13]. The compensation network design is analyzed in the paper.
Good performances in terms of noise and power consumption are achieved and the bandwidth limitations inherent to chopper modulation are removed. However, a very large die area is required (1.7 mm^2). Furthermore, the complexity of the architecture and of the compensation network make this solution unpractical.

Auto correction feedback loop for ripple suppression

A somehow similar solution is proposed in [3.14]. To avoid ripple appearing at the output, the amplifier offset is nulled before modulation, by means of an auto correction feedback loop. The principle of operation is shown in Fig. 3.12. In addition to the traditional two-stage chopper amplifier, a local feedback,

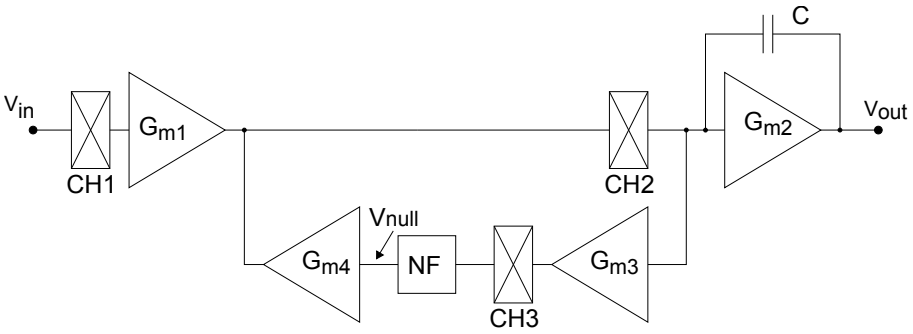

Figure 3.12: Auto correction feedback loop proposed in [3.14].

consisting in G_{m3}, G_{m4}, the notch filter NF and CH3, is implemented. This loop eliminates the offset of G_{m1}: G_{m3} senses the offset ripple after CH2. This component is then down-converted to DC by CH3, operating at f_{ch} like CH1 and CH2. This DC component passes through the switched capacitor notch filter (more details in the paper) and gives raise to a voltage V_{null}. Through G_{m4} a feedback loop coupled to the output of G_{m1} is built. Thanks to the negative feedback, any offset DC current at the output of G_{m1} itself is nulled by G_{m4}. In this case, offset ripple is sensed at the input of the second-stage instead that at the output as in the case of the RRL of [3.11]. The loop gain results then to be independent from the output load or the amplifier closed-loop gain.
On the other hand, the notch filter NF selects the offset ripple avoiding to create disturbances on the input signal. Assuming a DC input, after CH2 we still have a DC signal. This signal is up-converted by CH3 and rejected by NF, designed to have the notch at f_{ch}.
The proposed technique has been used to design a three stage general purpose operational amplifier. A multi-path topology has been adopted in order to increase the available bandwidth and a nested-Miller frequency compensation scheme has been used. The author reports good results: autocorrection feedback loop achieves a 45 dB ripple rejection without impacting noise performances, power dissipation or die area. Low residual offset is also reported (1.3 µV). Main drawbacks of this technique are represented by the high loop gain required, since the ripple is sensed at a virtual ground node, and the presence of a switched capacitor filter, that could degrade noise performances, at least up to a certain point. The proposed technique could be exploited also in CFIA or 3-op-amp instrumentation amplifiers.

3.3.3 Mixed approaches for instrumentation amplifier design

Alternative approaches to overcome the offset ripple issue inherent with the chopper modulation have been proposed in the literature and often relies on Autozero to compensate for the input offset. Rather than modulating the offset, it is sampled and subtracted, in order not to generate ripple and to obtain a clean output.

An interesting solution is proposed by Pertijs and Kindt in [3.7]. A ping-pong autozeroed CFIA using chopper modulation to decrease input noise PSD is proposed. Fig. 3.13 shows the CFIA architecture, the timing diagram of the necessary phases and the input noise PSD in case chopping frequency $f_{ch} = 2f_{AZ}$ where f_{AZ} is the autozero frequency. Autozeroing has been adopted since it can provide a clean output and does not originate offset ripple. Ping-pong input topology is necessary to guarantee continuous time operation. The traditional way to implement AZ uses input capacitors to sample input offset. However, switch charge injection and kT/C noise limit the efficiency of this technique. In this work, offset is stored at the input of the additional transconductor g_{AZ}. During the zeroing phase ϕ_Z, g_{in} and g_{fb} inputs are shorted and an offset current appears at their outputs, which is fed into the integration capacitor C_{AZ}. The voltage on C_{AZ} is converted into a current by g_{AZ} so as to generate a compensating current that cancels the offset current. The loop gain of this offset-nulling loop suppresses the offset. During the amplification phase ϕ_A, C_{AZ} is disconnected. As a result, the stored correction voltage is maintained and g_{AZ} still compensate for the input offset. Input and feedback voltages are now connected to g_{in} and g_{fb}, respectively. The "pong" stage comprises an additional set of input and feedback transonductors with nulling circuitry and is operated at opposite clock phases, so that one stage amplifies the signal while the other is zeroed. Continuos-time operation is then achieved at the cost of doubled area and power consumption.

As described in Chap. 2, autozero approach increases the low-frequency noise, due to undersampling of thermal noise PSD. Typically, the bandwidth of the nulling loop f_{null} exceeds f_{AZ}, in order to let the nulling voltage to correctly settle in a single phase. The resulting input noise PSD will be a multiple of the thermal noise level of the transconductors. A possible solution to this issue is applying chopper modulation at a frequency above f_{AZ}, in order to up-convert the input noise PSD. This technique has been firstly introduced in [3.15] and is represented in Fig. 3.13(a), where it is operated at $2f_{AZ}$ [Fig. 3.13(b)]. The

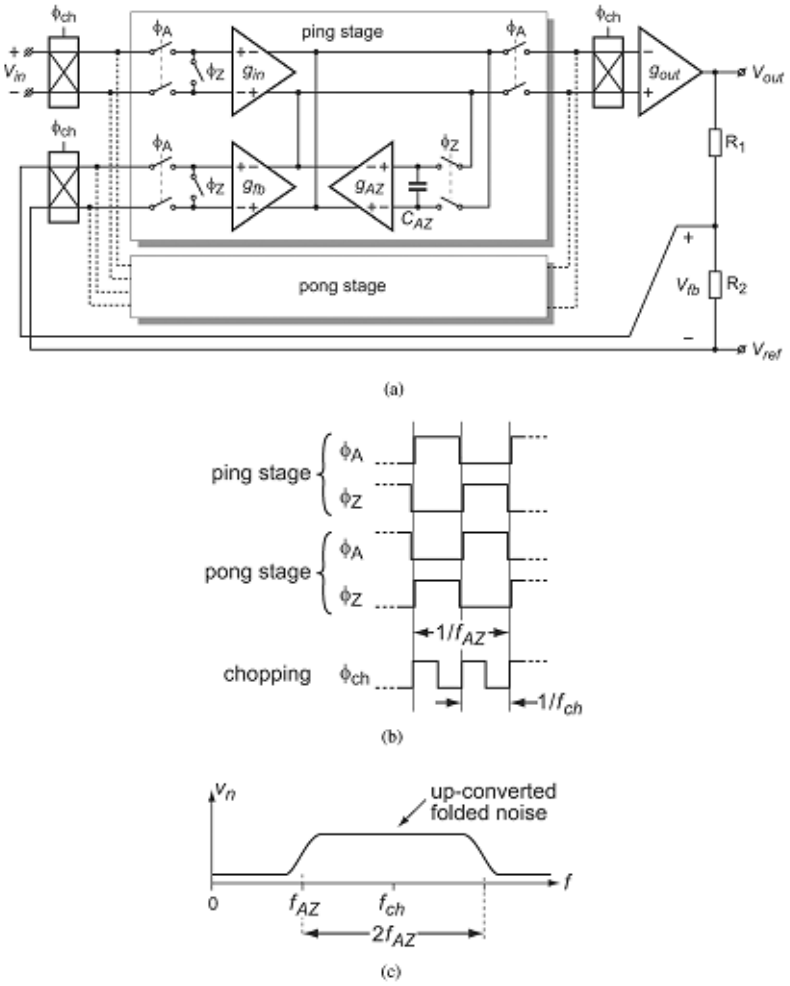

Figure 3.13: Architecture of the proposed ping-pong autozeroed CFIA chopped at $f_{ch} = 2f_{AZ}$: (a) block diagram; (b) phases; (c) input noise PSD, after [3.7] (© [2010] IEEE).

undersampled noise it up-converted to around $2f_{AZ}$, while the original white-noise PSD around $2f_{AZ}$ is down-converted to DC [Fig. 3.13(c)]. By this way, a ripple-free CFIA with same low-frequency PSD of the input transconductors is obtained. This approach is effective in solving noise problems but due to the switching during ϕ_A extra glitches due to the finite bandwidth of the transconductors are originated. Extra glitches can be avoided choosing f_{ch} smaller than f_{AZ}, e.g. $f_{AZ}/2$. By this way, chopping coincides with transitions from ϕ_{AZ} to ϕ_A and glitches are eliminated. In typical AZ amplifiers however this does not give any advantage in terms of noise since noise PSD at f_{ch} is not low. The authors show that employing a slow-settling nulling loop the bandwidth over which noise PSD is increased can be reduced. If f_{null} is chosen lower than $f_{AZ}/2$, the PSD near DC can be reduced to the transconductors PSD. As a consequence, the nulling loop takes more than one cycle to settle. This is not a problem since the integrator state is maintained from a cycle to the following one.

With this technique and choosing a small f_{null}, by means of chopping at $f_{AZ}/2$ it is possible to obtain the same input noise PSD of the transconductors, i.e. if no autozero is applied. More details can be found in the paper [3.7].

This technique has been used to design a three-stage nested-Miller compensated CFIA. Thanks to a careful design of the transconductors and to the adoption of trimming, an high gain accuracy (0.1 %) has been achieved, as well as an extremely high CMRR (140 dB). The noise PSD is relatively low (27 nV/$\sqrt{\text{Hz}}$) but due to the ping-pong input stage current consumption is also high (1.8 mA) and die area is increased (not reported).

A significant performance improvement can be achieved with the so-called "ping-pong-pang" technique [3.16]. In this approach, three transconductors are used: two are used for amplifying input and feedback, while the third is autozeroed. Then, transconductors change places in order to regularly compensate each of them. The architecture of the proposed three-stage ping-pong-pang CFIA is shown in Fig. 3.14. Another advantage of this technique is represented by the fact that each transconductor occupies a different position each third of the period. By this way, dynamic element matching is implemented and a very high gain accuracy can be achieved.

The transconductor are autozeroed once every 3 clock cycles ($f_{AZ} = f_{PPP}/3$ by means of a zeroing loop similar to that described in the previously discussed solution. The resulting low-frequency noise is up-converted by chopping modulation, with $f_{ch} = 1.5f_{AZ} = 2f_{PPP}$. With this choice, chopping coincides with the switching necessary to implement the ping-pong-pang and causes no extra

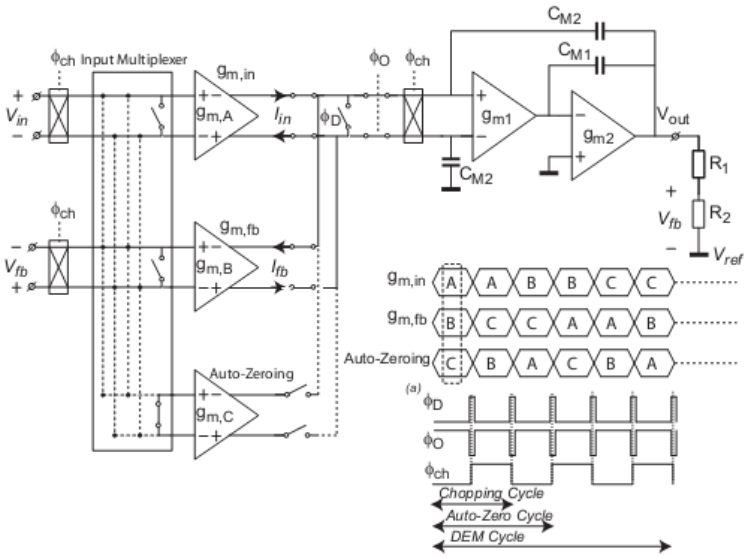

Figure 3.14: Architecture of the ping-pong-pang CFIA proposed in [3.16] (© [2011] IEEE).

glitches. Guard phases have also been added to prevent extra spikes associated with the transconductor DEM.

Good performances have been obtained: a noise PSD of 28 nV/$\sqrt{\text{Hz}}$ has been obtained, together with a very high gain accuracy (0.04 % maximum error) and a worst-case offset of 4 µV. Major drawbacks are represented by the die area and current consumption: 1.5 mm^2 and 480 µA from a 3.3 to 5 V power supply, respectively.

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Chapter 4

An instrumentation amplifier for MEMS flow sensor interfacing

In the previous chapters, after introducing MEMS integrated flow sensors, techniques for cancelling DC offset and flicker noise have been reviewed, since they constitute the preferred approach for realizing high precision sensor interfaces. Some examples of low offset low noise instrumentation amplifiers proposed in the literature have been also briefly reviewed. In this chapter, a novel instrumentation amplifier for MEMS thermal sensor interfacing is presented. The amplifier has been developed aiming to realize an high accuracy compact cell to be embedded in complete systems integrating sensor and electronics. The adopted techniques and architectural choices will be discussed, as well as the circuit topology.

4.1 Design target and specifications

The instrumentation amplifier described in this chapter has been targeted to interface MEMS thermal flow sensors. Thus, design specifications have been obtained considering typical characteristics of this kind of sensors. Fig. 4.1 shows the lumped parameter simplified representation of a CMOS integrated thermal flow sensor. The sensor can be represented as a balanced voltage source V_d with a common mode voltage V_c (cold junction biasing voltage). The

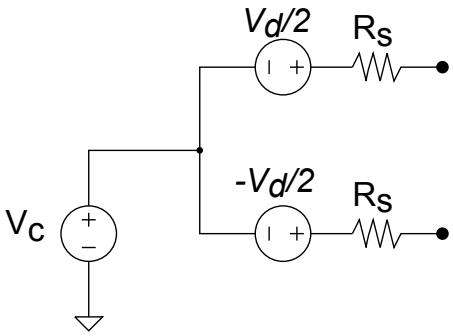

Figure 4.1: Simplified representation of a thermal calorimetric flow sensor

amplitude of V_d is usually limited to a few mV. The source series resistance R_s, split into two identical resistors, ranges from a few tens of kHz to a few MHz, due to the CMOS materials employed to build the thermopile, e.g. highly doped polysilicon. As described in Chap. 1, the sensor dynamic range is limited by the thermal noise associated with R_s. Thus, the amplifier should be designed to have an input equivalent noise resistance lower than R_s, provided that flicker noise is removed from base-band. The equivalent noise resistance R_{eq} can be defined as:

$$R_{eq} = \frac{S_{v-in}}{4kT} \tag{4.1}$$

where S_{v-in} is the input-referred thermal noise PSD of the amplifier. As an example, with $R_s = 100$ kΩ, an amplifier with $S_{v-in} < 40$ nV/$\sqrt{\text{Hz}}$, corresponding to $1.6 \cdot 10^{-15}$ V^2/Hz should be designed. The bandwidth of interest B of this kind of sensors is usually extended from DC to a few hundred of Hz. If $B = 200$ Hz and $S_{v-in} = 40$ nV/$\sqrt{\text{Hz}}$, the amplifier input-referred *rms* noise voltage results to be around 560 nV. The amplifier offset level should then be in the µV range.

Finally, since R_s is relatively large, an high amplifier input resistance is required in order to avoid gain attenuation. This is the typical case in CMOS instrumentation amplifiers.

Due to the low offset required, it is mandatory to adopt DOC (Dynamic Offset Cancellation) techniques to cancel input offset and strongly reduce the impact of $1/f$ noise. Among them, the best tradeoff between noise and power consumption is presented by chopper modulation. For this reason, this technique has been selected to design the proposed amplifier.

However, chopper modulation introduces some issues to be taken into account. First of all, offset ripple should be removed. As described in Chap. 3, ripple reduction introduces several architecture complications and tradeoffs, together

with silicon area increase due to the additional circuitry required. Here, an alternative approach to filter offset ripple will be presented.
Another often overlooked issue occurring in chopper amplifier is the input resistance decrease due to switching. This is particularly critical when high series resistance sensors have to be read, as in the case of CMOS thermal sensors. This aspect has been addressed and a novel solution, based on input and feedback port-swapping in a current-feedback instrumentation amplifier, has been proposed and will be described in the following. At the same time, the proposed solution also helps to increase the gain accuracy.

4.2 Port-swapping technique

In this section the techniques adopted to improve the perfomances of the proposed instrumentation amplifier will be presented.

4.2.1 Input impedance of a chopper amplifier

The switching operated by the input modulator in a chopper amplifier decreases the input impedance. This can be explained taking into account Fig. 4.2, showing a chopper modulated amplifier A with input capacitance C interfacing a balanced source V_d with series resistance R_s. This is the case of a CMOS thermal sensor interface. Switch arrays SA1-2 operate modulation and demodulation of the input signal. On the other hand, SA2 removes DC offset and $1/f$ noise shifting them to high frequencies, where they are rejected by the low pass filter LP. In the following analysis V_d is considered constant over a clock period T_{ch}.
The voltage V_{in} at the amplifier input is switched each phase by SA1 from V_d

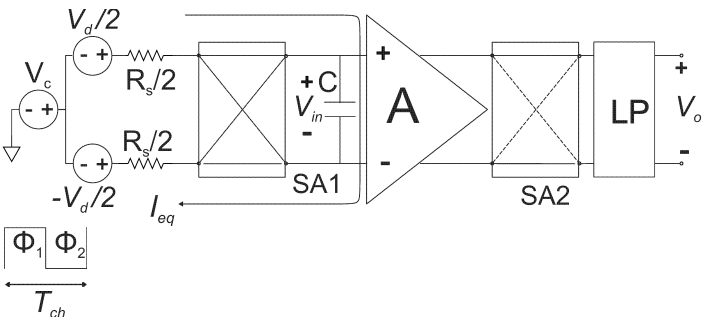

Figure 4.2: Chopper amplifier interfacing a balanced differential source with series resistance R_s.

to $-V_d$, or vice versa. Then, during the ϕ_1 phase, a total charge $Q = 2CV_d$ is transferred from V_d to C. The average current I_{eq} flowing in a clock period as indicated in Fig. 4.2, is given by:

$$I_{eq} = 4V_d C f_{ch} \tag{4.2}$$

where $f_{ch} = 1/T_{ch}$. The input resistance of the amplifier R_{in-ch} results then to be given by:

$$R_{in-ch} = \frac{1}{4Cf_{ch}} \tag{4.3}$$

In practical cases f_{ch} and C are strictly related to the equivalent input noise power spectral density (PSD) of the chopper amplifier S_v. Assuming that chopping occurs at frequencies lower than the corner frequency f_k, the latter can be written as:

$$S_v(f) \approx S_{v-in}(f_{ch}) \approx m\frac{K_F}{WL}\frac{1}{f_{ch}} \tag{4.4}$$

where S_{v-in} is the PSD of the amplifier A, K_F is the flicker noise coefficient, W and L are the width and length of the input transistors, respectively, and m is a coefficient greater than 1, depending on the amplifier topology. In order to reduce S_v, both f_{ch} and the device area WL should be increased. It should be also noted that C is proportional to WL. As a consequence, R_{in-ch}, which in the ideal case should be infinite, results to be decreased and a gain error is introduced. The relative gain error ϵ_{g-ch} is given by:

$$\epsilon_{g-ch} = \frac{A_d\left(V_d - V_{in}\right)}{A_d V_d} = 4R_s C f_{ch} \tag{4.5}$$

This error can be particularly detrimental if the source resistance R_s is high. If $C = 2.5$ pF, $f_{ch} = 40$ kHz and $R_s = 100$ kΩ, $\epsilon_{g-ch} = 4\%$. In this case, the equivalent input resistance $R_{in-ch} = 2.5$ MΩ. In addition, this error can be affected by process and temperature variations. Actually, the input capacitance C is largely process-dependent and increases with smaller oxide thickness t_{ox}, i.e. in more scaled processes, while R_s can be temperature-dependent, due to the sensor technology. This error is not acceptable for precise gain instrumentation amplifiers and has to be minimized.
Furthermore, Cf_{ch} is fixed by S_v through 4.4, considering that C is proportional to WL. On the other hand, it has been shown [4.1] that a precise relationship can be found between the gain error ϵ_{g-ch} and the minimum amplifier noise figure F achievable. In the following an approach capable to minimize the gain error related to C and R_s with no penalization in terms of input noise PSD

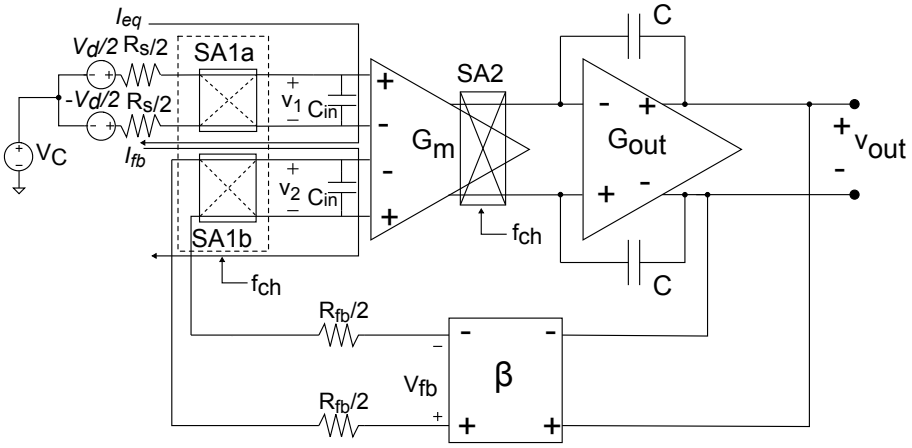

Figure 4.3: Chopper-modulated current feedback instrumentation amplifier.

will be described.

4.2.2 Input currents in a CFIA

The port-swapping technique proposed in this thesis is applied to instrumentation amplifiers with signal and feedback differential input ports. This technique has been previously proposed in [4.2, 4.3, 4.4] and used also in [4.5] as a viable approach to increase the gain accuracy of fully-differential chopper amplifiers. This feature will be described later.

To explain how the port-swapping technique operates in order to increase the input impedance of a fully-differential chopper amplifier, it is useful to recall the chopper CFIA described in the previous chapter and to make some considerations about the gain error introduced by the finite input impedance due to chopper modulation.

Fig.4.3 shows a chopper-modulated current feedback instrumentation amplifier interfacing a balanced differential source V_d, with series resistance R_s. Each input port has an input capacitance C_{in}. The gain is fixed by a resistive feedback network with feedback factor β and an output resistance R_{fb}, equally split on the two branches. Defining as g_{m1} and g_{m2} the transconductances of input and feedback ports, respectively, and assuming $g_{m1} = g_{m2}$ and defining as A the open loop voltage gain of the two-stage amplifier constituted by G_m and G_{out}, we obtain:

$$A_d = \frac{V_{out}}{V_d} = \frac{1}{\beta}\frac{1}{1+\frac{1}{\beta A}} \approx \frac{1}{\beta}\left(1-\frac{1}{\beta A}\right) \tag{4.6}$$

where A_d is the differential gain of the closed-loop amplifier. The rightmost equation holds if $\beta A >> 1$. If this condition holds, $A_d \approx 1/\beta$.
Chopper modulation is performed by SA1a-b and SA2. The former modulate signal and feedback voltages, while SA2 performs signal demodulation and offset and $1/f$ noise modulation. Ripple filtering is achieved by the Miller's integrator, with the simplifying hypothesis that f_{ch} is much larger than f_p (see Eq. 3.27 and Sec. 3.3.1).
As in the case discussed in Sec. 4.2.1, the voltage on the input port, v_1, is switched from V_d to -V_d each phase, or vice versa, while v_2 is switched from V_{fb} to $-V_{fb}$ or vice versa, where $V_{fb} = \beta V_{out}$. Due to the charge transfer on C_{in}, the average currents flowing through the input ports during a clock period T_{ch}, I_{eq} and I_{fb}, as indicated in the figure, are given by the following equations, respectively:

$$I_{eq} = 4V_d C_{in} f_{ch} \tag{4.7}$$

$$I_{fb} = 4V_{fb} C_{in} f_{ch} \tag{4.8}$$

Then, the average values of v_1 and v_2 can be calculated:

$$\overline{v_1} = V_d \left(1 - 4R_s C_{in} f_{ch}\right) \tag{4.9}$$

$$\overline{v_2} = V_{fb} \left(1 - 4R_{fb} C_{in} f_{ch}\right) = \beta V_{out} \left(1 - 4R_{fb} C_{in} f_{ch}\right) \tag{4.10}$$

Hypothesizing an ideal ripple filtering operated by the integrator, V_{out} coincides with its average value $\overline{V_{out}}$. Therefore, in the following, V_{out} will be intended as its average value.
The amplifier gain A_d can then be calculated taking into account $\overline{v_1}$ and $\overline{v_2}$ and recalling that $V_{out} = A\left(\overline{v_1} - \overline{v_2}\right)$:

$$V_{out} = A\left[V_d \left(1 - 4R_s C_{in} f_{ch}\right) - \beta V_{fb} \left(1 - 4R_{fb} C_{in} f_{ch}\right)\right] \tag{4.11}$$

With simple calculations:

$$\begin{aligned} A_d = \frac{V_{out}}{V_d} &= \frac{A\left(1 - 4R_s C_{in} f_{ch}\right)}{1 + \beta A \left(1 - 4R_{fb} C_{in} f_{ch}\right)} \\ &= \frac{1}{\beta} \frac{1 - 4R_s C_{in} f_{ch}}{\frac{1}{\beta A} + \left(1 - 4R_{fb} C_{in} f_{ch}\right)} \\ &= \frac{1}{\beta} \frac{1 - 4R_s C_{in} f_{ch}}{1 - 4R_{fb} C_{in} f_{ch}} \frac{1}{1 + \frac{1}{\beta A \left(1 - 4R_{fb} C_{in} f_{ch}\right)}} \end{aligned} \tag{4.12}$$

If $\beta A >> 1$, as it is usually verified:

$$A_d \approx \frac{1}{\beta} \frac{1 - 4R_s C_{in} f_{ch}}{1 - 4R_{fb} C_{in} f_{ch}} \tag{4.13}$$

If $4R_{fb} C_{in} f_{ch} << 1$, using first order Taylor series expansion it is possible to write:

$$A_d \approx \frac{1}{\beta} \left(1 - 4R_s C_{in} f_{ch}\right) \left(1 + 4R_{fb} C_{in} f_{ch}\right) \tag{4.14}$$

and, neglecting second order terms, we finally obtain:

$$A_d \approx \frac{1}{\beta} \left[1 - 4C_{in} f_{ch} \left(R_s - R_{fb}\right)\right] \tag{4.15}$$

The relative gain error ϵ_{g-ch} introduced by the chopper modulation is then given by:

$$\epsilon_{g-ch} \approx -4C_{in} f_{ch} \left(R_s - R_{fb}\right) \tag{4.16}$$

Usually, R_{fb} is in the kΩ range, to minimize the thermal noise contribution of the feedback network and to make it negligible with respect to that of R_s. If CMOS flow sensors or other kind of thermopile-based thermal sensors are taken into account, R_s can be significantly larger than R_{fb}. In this case, ϵ_{g-ch} becomes equal to Eq. 4.5 and become relevant. A trivial solution to cancel out the gain error may be to make $R_s = R_{fb}$, adding two resistors in the feedback path. This solution is not acceptable, since it involves significant disadvantages:

- Introduction of a thermal noise source with a PSD comparable with the source resistors, with significant degradation in terms of dynamic range.
- The gain error is cancelled out only for a given value of R_s. This aspect leads to designs optimized only for a given sensor.

It is clear that this source of error in chopper amplifiers is more relevant in case of high series resistance sensors. Moreover, trade-offs between noise, area, gain accuracy and residual offset are introduced.

4.2.3 Port-swapping technique

In this section the port-swapping technique adopted to increase the chopper amplifier input resistance in order to improve the gain accuracy without degrading noise performances is presented.
Fig. 4.4a shows a chopper-modulated current-feedback instrumentation amplifier where the input modulators SA1a-b have been replaced by the single

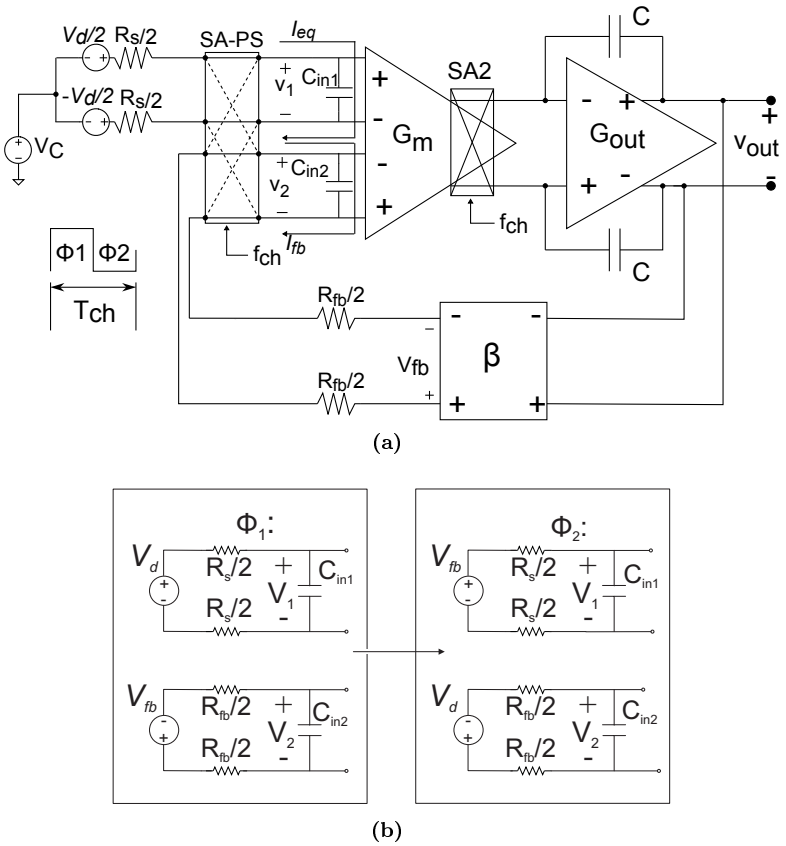

Figure 4.4: Chopper CFIA including port swapping modulation (a). The connection of V_d and V_{fb} during ϕ_1 and ϕ_2 are also shown (b).

modulator SA-PS. The latter swaps signal and feedback paths, both with sign inversion, as clarified in Fig. 4.4b. Capacitances C_{in1} and C_{in2} represent the input capacitance of signal and feedback paths, respectively. During ϕ_1, which lasts $T_{ch}/2$, V_d is straightly connected to the signal port, while V_{fb} is connected with sign inversion to the feedback port. At the end of ϕ_1, hypothesizing that $R_sC_{in} << T_{ch}$, $v_1 = V_d$ and $v_2 = V_{fb}$. During ϕ_2, V_d is connected to the feedback port with sign inversion while V_{fb} is straightly connected to the signal port. At the end of ϕ_2, with the same hypothesis, we have $v_1 = V_{fb}$ and $v_2 = V_d$. The sign inversion is guaranteed by the subtraction operated by the first stage G_m.

To understand how the technique increases the input impedance, it is possible

first to write v_1 and v_2 at the end of ϕ_1:

$$v_{Cin1} = v_1 = V_d \tag{4.17}$$

$$v_{Cin2} = v_2 = V_{fb} = \beta V_{out} \tag{4.18}$$

At the end of ϕ_2, it holds:

$$v_{Cin1} = v_1 = V_{fb} = \beta V_{out} \tag{4.19}$$

$$v_{Cin2} = v_2 = V_d \tag{4.20}$$

Thanks to the negative feedback, we also have:

$$\beta V_{out} = \frac{\beta A}{1 + \beta A} \tag{4.21}$$

where, again, A is the open-loop voltage gain of the two-stage amplifier. Then, it is possible to write the voltage variation Δv_1 and Δv_2 between the end of phase ϕ_2 and the end of phase ϕ_1:

$$\Delta v_1 = \beta V_{out} - V_d = \left(\frac{\beta A}{1 + \beta A} - 1 \right) V_d = -\frac{V_d}{1 + \beta A} \approx -\frac{V_d}{\beta A} \tag{4.22}$$

$$\Delta v_1 = V_d - \beta V_{out} = \left(1 - \frac{\beta A}{1 + \beta A} \right) V_d = \frac{V_d}{1 + \beta A} \approx \frac{V_d}{\beta A} \tag{4.23}$$

Assuming that $C_{in1} = C_{in2} = C_{in}$, the average current I_{eq} and I_{fb} flowing through the signal and feedback port, respectively, are given by:

$$I_{eq} = -\frac{2 C_{in} f_{ch} V_d}{\beta A} \tag{4.24}$$

$$I_{fb} = \frac{2 C_{in} f_{ch} V_d}{\beta A} \tag{4.25}$$

Then, averaging over a period:

$$\overline{v_1} = V_d \left(1 - \frac{2 R_s C_{in} f_{ch}}{\beta A} \right) \tag{4.26}$$

$$\begin{aligned} \overline{v_2} &= V_{fb} \left(1 + \frac{2 R_{fb} C_{in} f_{ch}}{\beta A} \right) \\ &= \beta V_{out} \left(1 + \frac{2 R_{fb} C_{in} f_{ch}}{\beta A} \right) \end{aligned} \tag{4.27}$$

As in the previous case, it is possible to obtain the differential gain starting from V_{out} (intended as the average value of the output voltage):

$$\begin{aligned} V_{out} &= A\left(\overline{v_1} - \overline{v_2}\right) \\ &= A\left[V_d\left(1 - \frac{2R_sC_{in}f_{ch}}{\beta A}\right) - \beta V_{out}\left(1 + \frac{2R_{fb}C_{in}f_{ch}}{\beta A}\right)\right] \\ &= \frac{AV_d\left(1 - \frac{2R_sC_{in}f_{ch}}{\beta A}\right)}{1 + \beta A\left(1 + \frac{2R_{fb}C_{in}f_{ch}}{\beta A}\right)} \end{aligned} \tag{4.28}$$

Thus:

$$\begin{aligned} A_d =& \frac{A\left(1 - \frac{2R_sC_{in}f_{ch}}{\beta A}\right)}{1 + \beta A\left(1 + \frac{2R_{fb}C_{in}f_{ch}}{\beta A}\right)} \\ =& \frac{1}{\beta}\frac{1 - \frac{2R_sC_{in}f_{ch}}{\beta A}}{1 + \frac{2R_{fb}C_{in}f_{ch}}{\beta A}}\frac{1}{1 + \frac{1}{\beta A\left(1 + \frac{2R_{fb}C_{in}f_{ch}}{\beta A}\right)}} \end{aligned} \tag{4.29}$$

Considering that $R_{fb} << R_s$ and $R_{fb}C_{in}f_{ch} << 1$, using first order Taylor expansion, the gain expression can be simplified:

$$A_d \approx \frac{V_d}{\beta}\left(1 - \frac{2R_sC_{in}f_{ch}}{\beta A}\right) \tag{4.30}$$

where $1/\beta$ is the ideal gain of the amplifier. The relative gain error can be written:

$$\epsilon_{g-ps} = \frac{2R_sC_{in}f_{ch}}{\beta A} \tag{4.31}$$

The error results to be reduced by a factor $2\beta A$ with respect to that occurring in the traditional chopper architecture. Since typical loop values ranges from several hundred to some thousands in typical instrumentation amplifiers, ϵ_{g-ps} results to be strongly reduced. This means that the input impedance of the amplifier has been boosted by the same factor and becomes:

$$R_{in-ps} = \frac{\beta A}{2C_{in}f_{ch}} \tag{4.32}$$

With the same values than in the simple chopper amplifier and a loop gain $\beta A = 500$, the input impedance results to be increased to 2.5 GΩ, which is a very high value.
Unfortunately, in practice, input offset and bias currents are still present due

to modulator non-idealities, such as charge injection and clock feedthrough. At the same time, input impedance is influenced by bond pads, PCB wiring and chopper clock rise/fall edges and will be therefore degraded [4.6]. These effects can be limited using low chopper frequencies.
However, port-swapping technique allows to increase the intrinsic input resistance of a chopper amplifier, enabling the design of very high input impedance low-offset instrumentation amplifiers.

Dynamic element matching

Another important feature of port-swapping technique when applied to current feedback or other kinds of instrumentation amplifiers is the ability of performing dynamic element matching between the input ports.
Let us recall Eq. 3.23:

$$A_d = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m2}} \frac{1}{\beta} \tag{4.33}$$

If $g_{m1} = g_{m2}$, A_d becomes $1/\beta$. Otherwise, if a mismatch between g_{m1} and g_{m2} is present, it directly causes a gain error of the same amount. When dealing with CMOS transconductors, the g_m mismatch between two differential pairs can easily reach 1-5 %, due to transistor and tail current source mismatches. This error cannot be accepted in high precision instrumentation amplifiers.
With reference to Fig. 4.4a, during ϕ_1 v_{in} is connected to the signal port, with transconductance g_{m1} and v_{fb} to the feedback port, with g_{m2}. During ϕ_2, v_{in} is connected to the signal port while v_{fb} to the input port. Defining $g_{m1} = g_m + \Delta g_m/2$ and $g_{m2} = g_m - \Delta g_m/2$, we obtain during ϕ_1:

$$A_{d1} = \frac{1}{\beta} \frac{g_m + \frac{\Delta g_m}{2}}{g_m - \frac{\Delta g_m}{2}} \tag{4.34}$$

and during ϕ_2:

$$A_{d2} = \frac{1}{\beta} \frac{g_m - \frac{\Delta g_m}{2}}{g_m + \frac{\Delta g_m}{2}} \tag{4.35}$$

The average gain $\overline{A_d}$ over a DEM period can be calculated:

$$\overline{A_d} = \frac{A_{d1} + A_{d2}}{2} = \frac{1}{2} \frac{1}{\beta} \left(\frac{g_m + \frac{\Delta g_m}{2}}{g_m - \frac{\Delta g_m}{2}} + \frac{g_m - \frac{\Delta g_m}{2}}{g_m + \frac{\Delta g_m}{2}} \right) \tag{4.36}$$

Assuming that $\Delta g_m/g_m << 1$ we obtain:

$$\overline{A_d} = \frac{1}{\beta}\left[1 + \frac{1}{2}\left(\frac{\Delta g_m}{g_m}\right)^2\right] \tag{4.37}$$

The relative gain error induced by the transconductor mismatch is then reduced from $\Delta g_m/g_m$ to $1/2(\Delta g_m/g_m)^2$. For a transconductance mismatch of 1-5%, this technique reduces the gain error to 0.01%-0.25%, which is more than one order of magnitude lower. As well as the offset ripple, the dynamic matching of the input transconductors originate an additional ripple. In this ideal case, this ripple is filtered by the Miller's integrator as well.

4.2.4 Common-mode related issues

A fully differential amplifier should be able to provide the output with a common-mode voltage (CM) chosen by the designer, which is not necessarily the same as the input CM. Actually, the input CM depends on the sensor and the instrumentation amplifier should be able to comply with it.
When port swapping technique is applied as discussed above, a possible source of error is represented by the difference between input and output CM. In this case, due to the action of the modulator SA-PS, each port (signal and feedback) experiences a different CM each clock phase. Making reference to Fig. 4.4a, the input CM is given by V_c and the output CM is defined as V_{co}. Furthermore, no common-mode level shift takes place into the feedback network. Then, the common-mode voltage of V_{fb} is still V_{co}. As clarified in Fig. 4.5, during ϕ_1 V_c

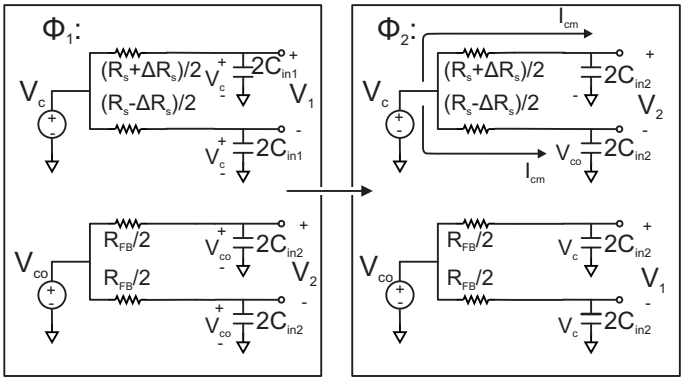

Figure 4.5: Common-mode voltages connection during ϕ_1 and ϕ_2.

is applied to the input port, while during ϕ_2 to the feedback port. Vice versa, V_{co} is applied during ϕ_1 to the feedback port and during ϕ_2 to the input port.

It should also be noted that here the differential input capacitances C_{in1} and C_{in2} have been replaced by the common-mode capacitances $2C_{in1}$ and $2C_{in2}$, on each input and feedback branch. It can be supposed that $C_{in1} = C_{in2} = C_{in}$. Due to switching, a common-mode current is supplied during ϕ_2 by V_c, in order to charge the input capacitances $2C_{in}$ of the feedback port from V_{co} to V_c. The average value I_{cm} of this current can be easily obtained:

$$I_{cm} = 4C_{in} f_{ch} \left(V_c - V_{co}\right) \tag{4.38}$$

The same current is supplied also during ϕ_1, since the input port has to switch during that phase from V_{co} to V_c. If a mismatch of the input resistances ΔR_s is present, an undesired differential signal originates, which adds up to the differential input V_d. With some calculations, we obtain that the output voltage due to CM and R_s mismatches is given by:

$$V_{out} = \frac{1}{\beta} \cdot 4C_{in} f_{ch} \Delta R_s \left(V_{co} - V_c\right) \tag{4.39}$$

It should be pointed out that also in this case V_{out} is intended as the output average voltage. Therefore, the undesired input differential voltage corresponding to this output is:

$$V_{d-cm} = 4C_{in} f_{ch} \Delta R_s \left(V_{co} - V_c\right) \tag{4.40}$$

If $C_{in} = 5$ pF, $f_{ch} = 40$ kHz, $\Delta R_s = 2$ kΩ and $(V_c - V_{co}) = 0.5$ V, $V_{d-cm} =$ 800 µV. This value is decisively not acceptable if signals with amplitude in the mV range have to be measured.

Moreover, input and feedback ports common-mode voltages have to settle in a time much smaller than $T_{ch}/2$, to avoid possible malfunctioning of the amplifier. This is not guaranteed if input and output CM voltages are very different and $R_s C$ is relatively large. This issue can become significant when low chopper frequencies are chosen (large input devices to minimize flicker noise at f_{ch}) and sensors with an high R_s, e.g. thermopiles, have to be interfaced.

An additional problem has been reported also in [4.5]. When port swapping is applied to a CFIA and input and output CM voltages are different, a gain error ϵ'_{cm}, not cancelled by port-swapping itself, originates. It can be written as:

$$\epsilon'_{g-cm} \approx \frac{\Delta g_m \Delta_{cm}}{2} + \Delta_{cm} \tag{4.41}$$

where Δg_m is the mismatch between the input transconductances when equal common-modes are applied and Δ_{cm} is the additional mismatch rising from the

difference between the common-modes. In the same paper, a possible solution employing class AB buffers to perform input devices substrate bootstrapping has been described.
The discussed issues cannot be neglected if the amplifier has to work with very different input and output common mode voltages. The proposed instrumentation amplifier employs a novel technique to overcome these issues.

4.3 Amplifier description

The proposed amplifier topology resembles the current-feedback instrumentation amplifier and is based on a 2$^{\text{nd}}$ order G_mC active filter architecture. To achieve low offset level, chopper modulation has been used, together with the described port swapping technique. A first version of the design has been presented in [4.2, 4.4]. An improved version has been discussed in [4.3]. In this thesis, the final version of the amplifier, including several significant refinements, will be presented.

4.3.1 Simplified architecture

The principle of operations can be explained making reference to Fig. 4.6, where the block diagram of a 2$^{\text{nd}}$ order low-pass filter (LPF) is shown. It consists of

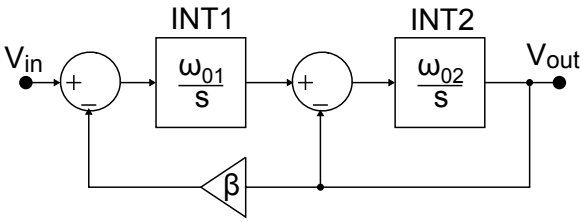

Figure 4.6: Second order LPF architecture.

two integrators, INT1 and INT2, with unity-gain angular frequencies ω_{01} and ω_{02}, respectively, and a resistive feedback network β. The transfer function of the filter, $H_{LP}(s)$, is given by:

$$H_{LP}(s) = \frac{A_0}{\frac{s^2}{\omega_c^2} + \frac{s}{\omega_0 Q} + 1} \tag{4.42}$$

where A_0 is the DC gain of the filter, ω_c the cut-off frequency and Q the quality factor. The relationship with ω_{01} and ω_{02} is given in Tab. 4.1. From

A_0	ω_c	Q
$1/\beta$	$\sqrt{\beta\omega_{01}\omega_{02}}$	$\sqrt{\beta\omega_{01}/\omega_{02}}$

Table 4.1: Second order LP filter characteristic parameters.

these relationships, we also obtain:

$$\omega_{01} = A_0 Q \omega_c \tag{4.43}$$

$$\omega_{02} = \frac{\omega_c}{Q} \tag{4.44}$$

Indicating with $S_{v1}(f)$ and $S_{v2}(f)$ the input noise PSD of INT1 and INT2, respectively, and with $S_{v\beta}$ the input noise PSD of the feedback network, the overall output noise PSD $S_{vout}(f)$ can be calculated with simple signal analysis:

$$S_{vout}(f) = |H_{LP}(f)|^2 \left[S_{v1}(f) + \beta^2 S_{v\beta}\right] + |H_{BP}(f)|^2 S_{v2}(f) \tag{4.45}$$

where $H_{BP}(s)$ is given by:

$$H_{BP}(s) = \frac{\frac{s}{\omega_c Q}}{\frac{s^2}{\omega_c^2} + \frac{s}{\omega_c Q} + 1} \tag{4.46}$$

Thus, INT2 input noise PSD results to be filtered by a pass-band function (H_{BP}), centred in ω_c, with unit maximum amplitude. In this way, INT2 offset is cancelled. At the same time, also low frequency noise is filtered and reduced. It should be noted that while H_{BP} has maximum amplitude of 1, H_{LP} has a maximum amplitude of $A_0 = 1/\beta$ and is typically $>> 1$. Besides, if the feedback network is resistive, $S_{v\beta}$ is only thermal. As pointed out before, the feedback network is sized to give a small noise contribution to avoid degrading overall noise performances. For these reasons, the main contribution to the output noise can be ascribed to INT1. Therefore, dynamic offset cancellation technique, i.e. chopper modulation, can be applied to this block. Particular care has to be devoted to the design of this integrator to obtain good system performances. In the following, it will be clarified that offset ripple originated by applying chopping to INT1 is filtered by $H_{LP}(s)$ as well. Then, a proper choice of the chopper frequency f_{ch} and the filter cut-off frequency $f_c = \omega_c/2\pi$ allows offset ripple to be rejected with no need of additional filters.

4.3.2 G_mC implementation

A viable approach to implement the described architecture is using G_mC integrators to build INT1 and INT2. Unfortunately, fully integrated G_mC integrators for low frequency applications are intrinsically characterized by relatively large thermal noise spectral densities and large silicon area. The typical topology of a G_mC integrator is shown in Fig. 4.7(a). The unity gain frequency of

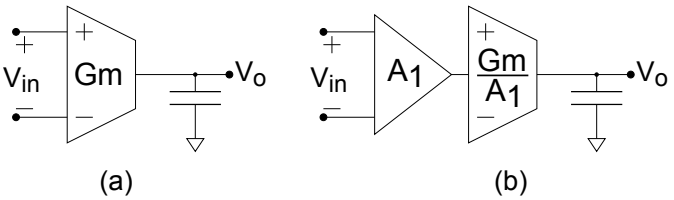

Figure 4.7: G_mC integrators based on simple transconductor (a) and two-stage transconductor (b).

this integrator is given by:

$$f_0 = \frac{G_m}{2\pi C} \tag{4.47}$$

where G_m is the transconductance of the transconductor. The latter has usually a single gain stage, where the input voltage is converted into a current, which is routed to the output port. The thermal component of the input noise PSD can be written as [4.7]:

$$S_{v-th} = m\frac{4kT}{G_m} \tag{4.48}$$

where m is a topology dependent factor greater than 1. The other important factor to be considered is the silicon area necessary to implement very small unity gain frequencies. They can be obtained either by integrating large capacitors or very low transconductances. The former solution obviously leads to a fast increase of the area occupation. The latter, on the other hand, can be easily explained: when a G_m as low as to obtain f_0 in the order of a few hundred Hz is required, the transconductor MOS aspect ratio (W/L) should be much smaller than 1. This can be obtained keeping W at the minimum allowed by the process and increasing the length L. In this condition, lower G_m means larger area. It can be easily shown that for a very small G_m, area becomes inversely proportional to transconductance.
In this condition, the integrator area can be written as:

$$A_{int} = k_G\frac{1}{G_m} + k_C C \tag{4.49}$$

where the first and second term in the right hand side are transconductor and capacitor area, respectively. Parameter k_C is a process dependent constant, while k_G depends also on the circuit topology. If, for simplicity, the transconductor is reduced to a single differential pair in saturation region, it can be written:

$$G_m = 2\mu C_{ox} \frac{W_{min}^2}{2W_{min}L} (V_{GS} - V_{TH}) \tag{4.50}$$

where W_{min} is the minimum allowed width. If the pair area $2W_{min}L$ is considered, k_G becomes:

$$k_G = 2\mu C_{ox} W_{min}^2 (V_{GS} - V_{TH}) \tag{4.51}$$

Note that G_m and C are tied by the relationship $G_m/2\pi C = \omega_0$, where $\omega_0 = 2\pi f_0$. Then, A_{int} results to be minimized when:

$$G_m = \sqrt{\frac{\omega_0 k_G}{k_C}} \tag{4.52}$$

The implications of Eq. 4.52 can be easily understood by means of a numerical example. Considering the target application (MEMS thermal sensors), assuming $Q = 1/\sqrt{2}$ (Butterworth transfer function), $f_c = 200$ Hz and $A_0 = 200$, we obtain $\omega_{01} = 178 \cdot 10^3$ rad/s from Eq. 4.44. We consider also $k_C = 2 \cdot 10^{14}$ µm^2/F and, with $\mu C_{ox} = 1 \cdot 10^{-4}$ A/V^2, $W_{min} = 0.5$ µm, $V_{GS} - V_{TH} = 0.1$ V, $k_G = 5 \cdot 10^{-6}$ µm$^2/\Omega$. The optimum G_m obtained with this values is 66 nS.
Using this value in Eq. 4.48 with $m = 1$ (optimistic case) we obtain $S_{v-th} = 500$ nV/$\sqrt{\text{Hz}}$, which is largely unacceptable for high precision instrumentation amplifier. This noise value can be reduced increasing G_m and, in turn, C. This approach is sub-optimal and can easily lead to too large integrator areas. The problem could even be worse in case of lower DC gains, since ω_{01} would further decrease.
A possible alternative is represented in Fig. 4.7(b), where a 2-stages G_mC integrator is represented. The single-stage transconductor is in this case preceded by a voltage amplifier with finite gain A_1. The same overall transconductance is maintained by choosing G_m/A_1 as transconductance of the actual transconductor stage. This leads to an increase of the noise PSD of the transcondcutor itself of the same factor A_1, according to Eq. 4.48. However, the PSD is referred to the input of the amplifier divided by A_1^2, so that a net noise reduction of A_1 is operated with respect to the single-stage case. Clearly, also the amplifier contributes to the total noise PSD. However, its thermal noise is not tied to

the unity gain frequency of the transconductor and can be decreased with no particular penalization in terms of silicon area, at the expense of power consumption.
However, integrator area is increased by A_1. It is possible to find the optimum A_1 value to minimize the overall integrator area, now given by:

$$A_{int} = k_G \frac{A_1}{G_m} + k_C C \tag{4.53}$$

The input noise PSD becomes:

$$S_{v-th} = m \cdot \frac{4kT}{A_1 G_m} \tag{4.54}$$

Hypothesizing that $m = 1$, we can obtain the optimum gain:

$$A_{1-opt} = \sqrt[3]{\frac{k_C}{\omega_0 k_G}\left(\frac{4kT}{S_{v-th}}\right)} \tag{4.55}$$

Using the same parameters as before and imposing $S_{v-th} = 20\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, the optimum gain A_{1-opt} turns out to be 70. This value is far from the initial single-stage case where $A_1 = 1$. This means that for a given noise value, the pre-amplification approach is more effective in minimizing the integrator area, with respect to the simple G_m increase.

4.3.3 Fully-differential implementation

A fully-differential G_mC implementation of the proposed instrumentation amplifier based on the active filter topology described above is shown in Fig. 4.8. The transconductors G_{m1a} and G_{m1b}, together with the load represented by G_{m2}, constitute a finite gain preamplifier. Hypothesizing that $g_{m1a} = g_{m1b} = g_{m1}$ (transconductances of G_{m1a} and G_{m1b}), the gain of the preamplifier is given by $A_1 = g_{m1}/g_{m2}$. With this choice, the preamplifier gain results to be a ratio of homogeneous quantities, therefore less sensitive to process and temperature variations.
The transconductor G_{m3} and the capacitances C_1 constitute the second stage of the two-stages G_mC integrator INT1. On the other hand, G_{m4a} and G_{m4b}, together with the operational amplifier OA and the Miller's capacitors C_2, constitute the second integrator INT2.
The feedback network is resistive and implemented by R_1 and R_2. The feedback

factor β is given by:

$$\beta = \frac{R_1}{2R_2 + R_1} \tag{4.56}$$

Thus, feedback voltage V_{fb}, results to be given by:

$$V_{fb} = \beta V_{out} \tag{4.57}$$

and the ideal DC gain of the preamplifier A_0:

$$A_0 = \frac{1}{\beta} \tag{4.58}$$

Actually, the amplifier working principle is similar to a Current-Feedback Instrumentation Amplifier. The first stage operates a voltage-to-current conversion by means of transconductors. The negative feedback drives the output voltage V_{out} in order to nullify I_{o1}, which is the output current of the first integrator.

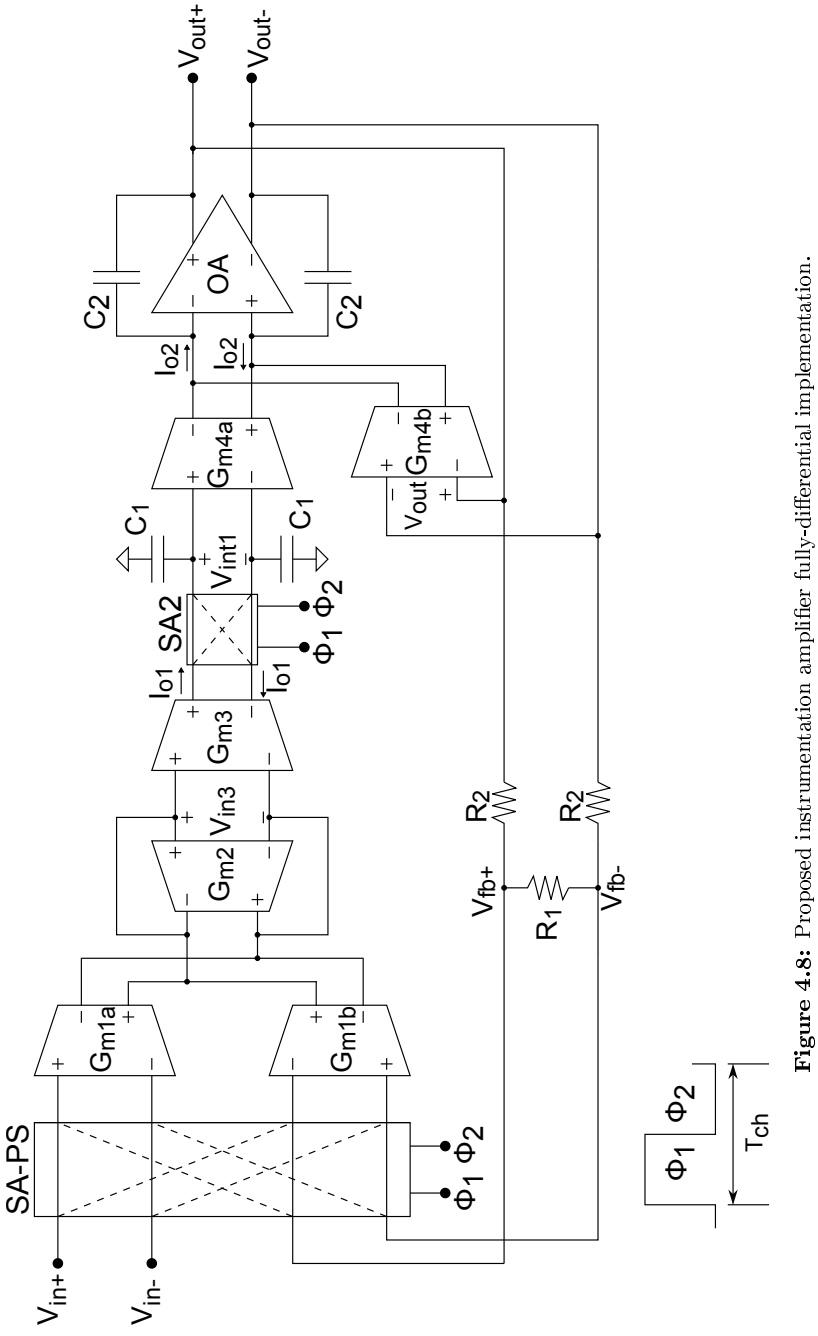

Figure 4.8: Proposed instrumentation amplifier fully-differential implementation.

However, the main difference from a simple CFIA resides in the improved filtering capability, obtained inserting the second integrator INT2 into the signal path. This solution allows offset ripple to be intrinsically rejected and the band of the amplifier to be properly limited to the low frequencies of interest for the target applications (MEMS thermal sensors).

Chopper modulation and port swapping

As widely explained in the previous section, the main contribution to offset and noise performances of the amplifier has to be ascribed to the first integrator. Therefore, chopper modulation has been applied to this block. Modulator SA2 shifts the offset and flicker noise of the amplifier around f_{ch} and its odd harmonics. This originates the described offset-ripple. However, this disturbance experiences the same transfer function H_{LP} of the signal. This can be explained as follows: hypothesizing that the first integrator has a constant transconductance over frequency, at least until several harmonics of f_{ch}, the effect on the output due to the square-wave modulated integrator output current is the same occurring when a square-wave voltage of amplitude $I_{o1}/(A_1 g_{m3})$, where g_{m3} is the transconductance of G_{m3}, is applied to the input and no chopper modulation takes place. Therefore, it is clear that offset ripple originated by the modulated offset is rejected or strongly attenuated by H_{LP}, since it experiences the same transfer function than the signal.
On the other hand, the input modulator SA-PS operates both sign inversion and port-swapping between signal and feedback paths at frequency f_{ch}. The modulator connects v_{in} to the signal port (G_{m1a}) and v_{fb} to the feedback port (G_{m1b}) straightly during phase ϕ_1. During phase ϕ_2 the modulator connects v_{in} to the feedback port with sign inversion and v_{fb} to the input port, again with sign inversion. The sign inversion is necessary to correctly implement chopper modulation. The port-swapping has been described before as a practical approach to increase the input impedance and compensate for gain errors due to input port mismatches. In this case, port-swapping operates the equalization of the signal and feedback preamplifier path gains, i.e. g_{m1a}/g_{m2} and g_{m1b}/g_{m2}, since the actual transconductance stage, G_{m3} is common to both paths. The principle of operation of this technique has been extensively described in the previous section. The port-swapping techniques originates a gain ripple, which is rejected by the filtering transfer function of the amplifier, as well as offset ripple.
It should be also recalled that the offset due to INT2 is strongly reduced by

the pass-band function $H_{BP}(s)$. Therefore, no modulation has been applied to this block.

Transfer function and filter parameters

The proper sizing of the amplifier transfer function $H_{LP}(s)$ can be achieved once the relationship between circuit parameters, such as capacitances and transconductances, and filter parameters, such as ω_c and Q, are established. It should be noted that in the following analysis chopper modulation is considered to be disabled and the following hypothesis hold:

$$g_{m1a} = g_{m1b} = g_{m1} \tag{4.59}$$

$$g_{m4a} = g_{m4b} = g_{m4} \tag{4.60}$$

The voltage V_{int1} is given by:

$$V_{int1}(s) = \frac{2}{C_1}\frac{I_{o1}}{s} \tag{4.61}$$

where $I_{o1} = g_{m3}V_{in3}$. Therefore:

$$V_{int1} = \frac{2}{C_1 s} g_{m3} V_{in3} \tag{4.62}$$

where:

$$V_{in3} = \frac{g_{m1}}{g_{m2}}\left(v_{in} - v_{fb}\right) \tag{4.63}$$

Then:

$$V_{int1} = \frac{2}{C_1 s} g_{m3} \frac{g_{m1}}{g_{m2}}\left(v_{in} - v_{fb}\right) = \frac{2}{C_1 s} A_1 g_{m3}\left(v_{in} - v_{fb}\right) \tag{4.64}$$

Then, the first integrator unity gain frequency ω_{01} results to be given by:

$$\omega_{01} = 2A_1\frac{g_{m3}}{C_1} \tag{4.65}$$

With similar calculations, it can be obtained:

$$V_{out} = 2\frac{g_{m4}}{C_2 s}\left(V_{int1} - V_{out}\right) \tag{4.66}$$

The second integrator unity gain frequency ω_{02} is then given by:

$$\omega_{02} = 2\frac{g_{m4}}{C_2} \tag{4.67}$$

Combining Eqns. 4.64 and 4.66 and with simple algebraic steps, it can be obtained:

$$H_{LP}(s) = \frac{V_{out}(s)}{v_{in}(s)} = \frac{1}{\beta} \frac{1}{\frac{C_1 C_2 s^2}{4A_1 g_{m3} g_{m4}} + \frac{C_1 s}{2A_1 g_{m3} \beta} + 1} \tag{4.68}$$

The transfer function parameters can then be easily obtained:

$$A_0 = \frac{1}{\beta} \tag{4.69}$$

$$\omega_c = \sqrt{4\beta A_1 \frac{g_{m3}}{C_1} \frac{g_{m4}}{C_2}} \tag{4.70}$$

$$Q = \sqrt{\beta A_1 \frac{g_{m3}}{C_1} \frac{C_2}{g_{m4}}} \tag{4.71}$$

The cut-off frequency $f_c = \omega_c / 2\pi$ and the quality factor Q can then be obtained at the design phase with proper choices of the circuit parameters.

DC analysis

In the previous section infinite DC gain of the transconductors has been assumed. This means that infinite output resistances have been assumed. Removing this hypothesis, it is possible to calculate the gain error due to finite loop gain of the amplifier. Let us define the DC gain of G_{m3}, A_3, as $g_{m3} r_{o3}$, where r_{o3} is the output resistance of G_{m3}, the DC gain of $G_{m4a,b}$, A_4, as $g_{m4} r_{o4}$, where r_{o4} is the output resistance of $G_{m4a,b}$ and A_{OA} as the DC gain of the operational amplifier OA. It can be obtained that at DC it holds:

$$\frac{V_{out}}{v_{in}} = \frac{A_1 A_3 A_4 A_{OA}}{1 + A_4 A_{OA} + \beta A_1 A_3 A_4 A_{OA}} = \frac{A_1 A_3 A_4 A_{OA}}{1 + A_4 A_{OA} (1 + \beta A_1 A_3)} \tag{4.72}$$

which, if $A_4 A_{OA} >> 1$, becomes:

$$\frac{V_{out}}{v_{in}} \approx \frac{A_1 A_3}{1 + \beta A_1 A_3} = \frac{1}{\beta} \frac{1}{1 + \frac{1}{\beta A_1 A_3}} \tag{4.73}$$

If $\beta A_1 A_3 >> 1$, first order Taylor expansion can be used:

$$\frac{V_{out}}{v_{in}} \approx \frac{1}{\beta} \left(1 - \frac{1}{\beta A_1 A_3} \right) \tag{4.74}$$

Thus, the gain error due to the finite loop gain is mainly determined by the first integrator DC gain. Therefore, it is important to implement this block with an high output resistance transconductor.

With a similar approach, it is possible to calculate the residual DC offset due to INT2 offset and finite DC gain of the integrators. Assuming that an offset V_{io2} is added at the input of G_{m4a}, it can be obtained:

$$\frac{V_{out}}{V_{io2}} = \frac{A_4 A_{OA}}{1 + A_4 A_{OA} (1 + A_1 A_3 \beta)} \tag{4.75}$$

that, if $A_4 A_{OA} >> 1$ and $\beta A_1 A_3 >> 1$, becomes:

$$\frac{V_{out}}{V_{io2}} \approx \frac{1}{\beta A_1 A_3} \tag{4.76}$$

which corresponds to an input-referred offset contribution of $V_{io2}/(A_1 A_3)$. Therefore, implementing G_{m3} with an high output resistance helps also in minimizing this offset contribution.

4.3.4 Common-mode related issues correction

In Sec. 4.2.4 a possible source of error has been highlighted. When the input common-mode voltage (CM) is different from the output CM, a significant gain error can arise if the source resistance is unbalanced. An effective solution to this issue, consisting in equalizing the input and feedback CM, has been developed. Fig. 4.9 shows the application of the proposed technique to the described instrumentation amplifier.

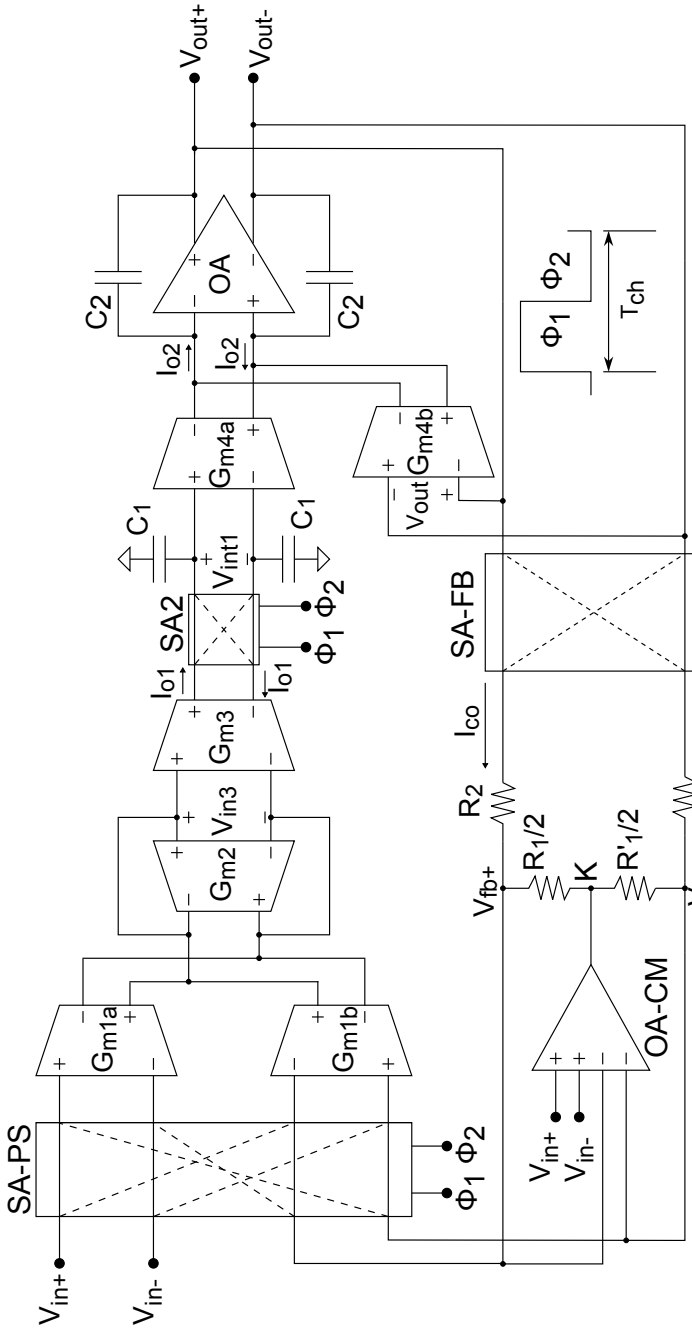

Figure 4.9: Common-mode related gain error correction.

The operational amplifier OA-CM calculates the input and feedback common-mode voltage, V_C and V_{Cfb}, respectively, and their difference. Then it drives the node K in order to equalize these CM voltages, by sinking or sourcing the common-mode current I_{co}, in order to translate V_{Cfb}. The loop gain A_{L-CM} is given by:

$$A_{L-CM} = A_{CM} \frac{R_2 + r_{out}}{R_1/2 + R_2 + r_{out}} \tag{4.77}$$

where has been hypothesized that $R_1'/2 = R_1/2$, $R_2' = R_2$ and where r_{out} is the amplifier output resistance. Since usually $R_1/2 << R_2 + r_{out}$, the loop gain becomes approximately A_{CM} where the latter is the open-loop gain of OA-CM. As a consequence, the error given by Eq. 4.40, results to be reduced by about A_{CM}.

This solution also cancels the gain error due to the transconductance mismatch introduced by the difference between input common-mode voltages (Eq. 4.41). The output common-mode of the amplifier is fixed by an internal common-mode feedback, while the input common-mode voltage depends on the sensor. These values can be different. Therefore, this solution adds flexibility to the amplifier in a very practical way. Moreover, since input and output CM are not expected to change during normal functioning of the amplifier, no particular specifications on the loop bandwidth are given. Therefore, the gain-bandwidth product of OA-CM can be made small, saving current. Its implementation will be shown in the following.

It should be noted that in Fig. 4.9 the input modulator SA-PS has been modified. The feedback voltage V_{fb} is now connected during ϕ_1 to G_{m1b} without sign inversion and during ϕ_2 to G_{m1a}, again without sign inversion. This operation is now implemented by SA-FB. This modification is necessary for the following reason. The feedback network in an actual realization is affected by mismatch. In this case, $R_1' \neq R_1$ and $R_2' \neq R_2$. If V_{CO} and V_C are different, OA-CM sinks (sources) the current I_{co}, as explained before.

Using the following positions and defining V_K as the voltage at node K:

$$\alpha = 1 - \beta \tag{4.78}$$

$$\beta' = \frac{R_1'}{2R_2' + R_1'} \tag{4.79}$$

$$\alpha' = 1 - \beta' \tag{4.80}$$

it can be obtained:

$$V_{fb+} = \beta V_{out+} + \alpha V_K \tag{4.81}$$

$$V_{fb-} = \beta' V_{out-} + \alpha' V_K \tag{4.82}$$

and:

$$V_{Cfb} = \frac{1}{2}\left[\left(\beta + \beta'\right) V_{CO} + \left(\alpha - \alpha'\right) V_K\right] \tag{4.83}$$

Since, thanks to the feedback loop, $V_{Cfb} \approx V_C$, we obtain:

$$V_K = \frac{V_C - \overline{\beta} V_{CO}}{\overline{\alpha}} \tag{4.84}$$

where $\overline{\beta} = \left(\beta + \beta'\right)/2$ and $\overline{\alpha} = \left(\alpha + \alpha'\right)$. On the other hand, if $V_{out} = 0$:

$$V_{fb} = \frac{\beta - \beta'}{\overline{\alpha}} \left(V_{CO} - V_C\right) \tag{4.85}$$

If the amplifier, as usual, has an high gain, then $\beta << 1$ and $\alpha \approx 1$. Therefore, considering a typical β mismatch $(\beta - \beta')$ of 1% and $(V_{CO} - V_C) = 1$ V, V_{fb} results to be 10 mV. If the modulator SA-PS shown in Fig. 4.8 is used, this undesired voltage component is treated as a signal, modulated and demodulated and appears at the output amplified, introducing then an error. If the modulator SA-PS structure of Fig. 4.9 is used, this component is indeed applied to G_{m1a} and G_{m1b} with the same sign and is therefore treated as an offset, shifted to high frequencies by SA2 and removed by $H_{LP}(s)$. The modulator SA-FB recovers the sign inversion necessary to maintain the negative feedback during ϕ_2.

4.4 Circuit implementation

The described architecture has been implemented using CMOS devices from the 3.3 V, 0.32 µm BCD6s (Bipolar-CMOS-DMOS) process from STMicroelectronics. The instrumentation amplifier has been targeted to interface MEMS flow sensors. Therefore, the specifications reported in Tab. 4.2 have been chosen. The amplifier transfer function cut-off frequency has been set to 200 Hz and the quality factor Q to $1/\sqrt{2}$ (0.707), corresponding to a Butterworth filter transfer function. The specified noise density S_v of 20 nV/$\sqrt{\text{Hz}}$ corresponds to an equivalent noise resistance of 24 kΩ and sets the resolution of the amplifier. The gain has been set equal to 201, choosing $R_2 = 200$ kΩ and $R_1 = 2$ kΩ.

Specifications	Value
f_c	200 Hz
Q	0.707
Gain	201
S_v	20 nV/$\sqrt{\text{Hz}}$
f_{ch}	20 kHz

Table 4.2: Amplifier specifications.

With this choice, the noise associated with the feedback network results to be negligible.
Considering the given specifications, it is possible to calculate the integrator unity gain pulsations, ω_{01} and ω_{02}:

$$\omega_{01} = 177.7 \cdot 10^3 \text{ rad/s} \tag{4.86}$$

$$\omega_{02} = 1777 \text{ rad/s} \tag{4.87}$$

Finally, chopper switches are operated at 20 kHz, to avoid the increase of residual DC offset due to charge injection.
In the following, the detailed circuit implementation will be presented.

4.4.1 Noise analysis

The noise specification requires a low-noise oriented design. To this purpose, it is important to identify the main noise contributions, in order to properly focus the design effort. Eq. 4.45 shows the noise contribution of the integrators and feedback network when the simplified block architecture is taken into account. However, when the input noise PSD of the actual amplifier implementation S_{v-in} is considered, additional noise contributions have to be analysed. Hereinafter, noise contribution of each block will be discussed:

- **Input modulator SA-PS:** the input modulator SA-PS implements both chopper modulation and port-swapping. The MOS switches are characterized by a r_{on} resistance. Therefore, the single switch contribution is given by $4kTr_{on}$. Since four switches are always in their on state, the total input noise PSD S_{v-sw} results to be $16kTr_{on}$.

- **Preamplifier ($\mathbf{G_{m1a}}, \mathbf{G_{m1b}}$ and $\mathbf{G_{m2}}$)**: the preamplifier contributes to the amplifier input noise with its input-referred noise PSD S_{v-pre}. Since chopper modulation is applied, its contribution at the frequencies of interest is then approximately given by $S_{v-pre}(f_{ch})$.

- **First integrator INT1 (G_{m3}):** the transconductor G_{m3} experiences chopper modulation and preamplification. Therefore, its noise PSD contribution S_{v-int1} to S_{v-in} at low frequencies has to be evaluated at f_{ch} and is referred to the input divided by A_1^2.

- **Second integrator INT2 ($G_{m4a,b}$ and OA):** the input noise PSD of the second integrator is processed by $H_{BP}(s)$. The resulting output PSD is then referred to the input divided by A_0^2. At low frequencies ($f < f_c$), the input PSD contribution S_{v-int2} results to be given by:

$$S_{v-int2}(f) = S_{v-gm4}(f) \left| \frac{f}{f_0 Q A_0} \right|^2 \tag{4.88}$$

  This contribution can be easily made negligible, since $|f/f_0 Q A_0|^2$ tends to 0 when $f << f_0$.

- **Feedback network:** the feedback network contribution S_{v-fb} to the amplifier noise PSD is given by $4kTR_{eq}$ where R_{eq} is the resistance seen looking towards the feedback network from the feedback port of the preamplifier and is given by $R_1//2R_2$. Since $A_0 = 1+2R_2/R_1 = 201$, $R_2 = 100R_1$. Therefore, $R_{eq} \approx R_1$ and $S_{v-fb} = 4kTR_1$. This contribution can be made negligible by choosing R_1 small enough. In our case, $R_1 = 2$ kΩ. Therefore, S_{v-fb} can be neglected.

- **Output modulator SA-FB:** the noise contribution due to the on-resistance of this modulator is not significant. Actually, the on resistance should be as lower than R_2 as not to decisively impact gain value. Besides, its noise contribution is multiplied by β being further reduced.

- **Common-mode loop operational amplifier (OA-CM):** the output voltage noise of OA-CM causes small fluctuations of node K voltage, which translate into small variations of the feedback voltage common mode. Since these variations are ineffective on the differential voltage v_{fb}, no effects on the differential mode voltage noise of the amplifier are originated. Therefore, at least when no mismatch is present, noise of OA-CM does not contribute to the amplifier voltage noise PSD.

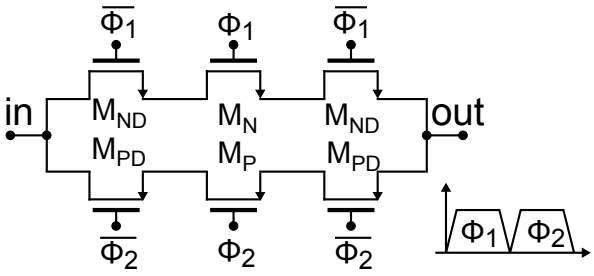

Figure 4.10: Input switch implemented with pass-gate and dummy switches.

Taking into account the previous analysis, the input noise PSD of the amplifier, S_{v-in}, can be estimated by:

$$\begin{aligned} S_{v-in}(f) &= S_{v-sw}(f) + S_{v-pre}(f_{ch}) + \frac{S_{v-int1}(f_{ch})}{A_1^2} + S_{v-int2}(f) \\ &= S_{v-sw}(f) + S_{v-pre}(f_{ch}) + \frac{S_{v-int1}(f_{ch})}{A_1^2} \\ &+ S_{v-gm4}(f) \left| \frac{f}{f_0 Q A_0} \right|^2 \end{aligned} \tag{4.89}$$

Eq. 4.89 highlights the main contributions to the input noise of the instrumentation amplifier, suggesting the proper design choices for minimizing the noise PSD.

4.4.2 Input modulator

The input modulator SA-PS implements both signal modulation and port swapping. The switches constituting the modulator have been carefully sized since they impact both input noise and residual offset, due to charge injection and clock feedthrough.

The input modulator has been implemented using pass-gates to increase the available input swing and dummy switches to reduce charge injection absolute value. As discussed before, this solution in ineffective on residual offset but helps to reduce the residual input offset current. This is particularly important in this design, since we are dealing with high series resistance sensors. Fig. 4.10 shows the input switch design. The size of M_N and M_P is $W = 30$ µm and $L = 0.5$ µm. The dummy switches M_{ND} and M_{PD} have same length and half width (15 µm). With this sizing the r_{on} of a single switch is around 226 Ω. Thus, since 4 switches are always in their on state at the same time, their input noise contribution is equivalent to a 900 Ω resistance, i.e. $0.15 \cdot 10^{-16}$

V^2/Hz corresponding to 3.9 $\text{nV}/\sqrt{\text{Hz}}$. If compared with the required input noise PSD (20 $\text{nV}/\sqrt{\text{Hz}}$), it results to be negligible.

4.4.3 Preamplifier design

As widely discussed above, the preamplifier decisively influences the noise performance of the instrumentation amplifier. The preamplifier gain also contributes to determine the filter parameters (ω_c, Q). The gain of the preamplifier can be optimized recalling Eq. 4.55. Using the same parameters of the example, which are still valid, but considering a larger overdrive for the transconductor transistors (0.5 V), the optimum gain A_{1-opt} turns out to be ≈ 125. However, in an actual implementation, m parameter is greater than 1. For this reason, the preamplifier gain has been chosen equal to around 600. With this choice, the unity gain frequency of the first integrator results to be 296.2 rad/s.
The preamplifier consists in a telescopic cascode single-stage amplifier. This configuration allows better noise performance to be achieved with respect to the folded cascode architecture, at the expense of reduced output swing. This is not a problem, since, thanks to negative feedback, the output of the preamplifier experiences only small variations. A differential load, constituted by devices M_{o1} and M_{o2} has been used, in order to ensure gain accuracy against process and temperature. This choice has been operated because filter parameters depends on A_1. Signal and feedback ports of the instrumentation amplifier are implemented by differential pairs M_1-M_2 and M_3-M_4, respectively. The bias PMOS current sources, M_{11} and M_{13}, are driven by a common-mode feedback, which sets V_{cmfb} in order to stabilize the common-mode voltage of the preamplifier at a given value V_{co-pre}. Fig. 4.11 shows the schematic of the preamplifier. The common-mode feedback, realized as a double differential pair OTA, is not shown. The Norton's output currents I_{out+} and I_{out-} originate from the input differential pairs and are given by:

$$I_{out+} = g_{mi}\left(\frac{v_{ad}}{2} + \frac{v_{bd}}{2}\right) \tag{4.90}$$

$$I_{out-} = -g_{mi}\left(\frac{v_{ad}}{2} + \frac{v_{bd}}{2}\right) \tag{4.91}$$

where g_{mi} is the trasconductance of M_1-M_4, $v_{ad} = v_{a+} - v_{a-}$ and $v_{bd} = V_{b+} - v_{b-}$. The load transistors M_{o1} and M_{o2} offer a differential resistance equal to $1/g_{mo}$ where g_{mo} is their transconductance. The cascode configuration of the input branch guarantees that, thanks to the high output impedance, the differential pair output current flows practically entirely into the low-impedance

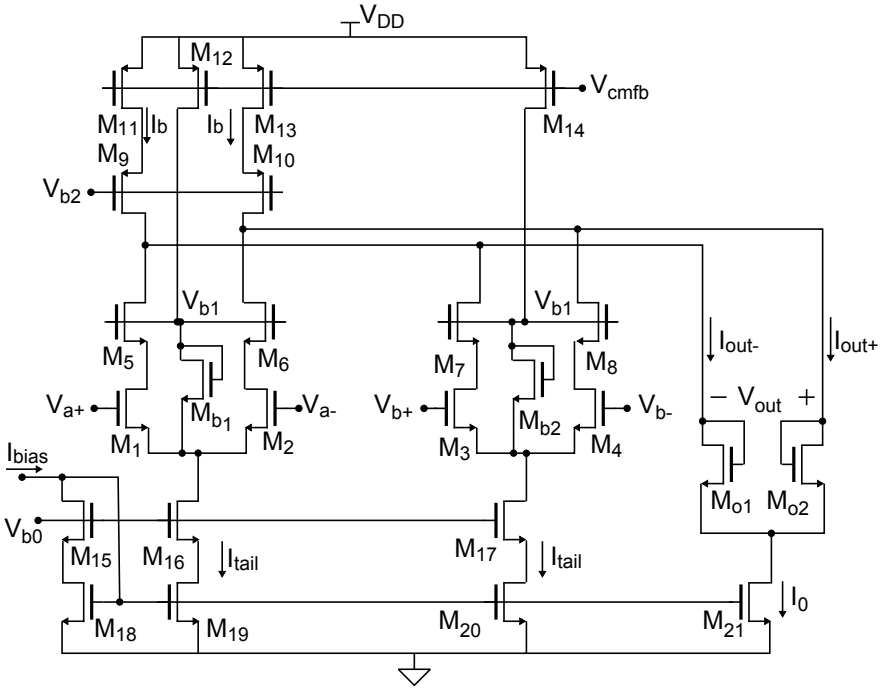

Figure 4.11: Preamplifier schematic.

differential pair. Therefore:

$$A_1 = \frac{g_{mi}}{g_{mo}} \tag{4.92}$$

The amplification results to be given by a transconductance ratio. The ratio between homogeneous quantities guarantees, at least at a first order, stability against process and temperature variations.

Transistors M_1-M_4 have been biased in sub-threshold region of operation, where the g_m/I_d ratio is maximum. In this region, the best trade-off between thermal noise and power consumption is achieved. On the other hand, the input linear range of a differential pair biased in weak inversion is quite small (around ± 40 mV). As discussed before, in the current-feedback instrumentation amplifier the input transconductor has the input voltage directly applied to its differential input. This can lead to THD degradation, especially for inputs in the order of a few tens of mV. However, the target application is characterized by sensor voltages in the order of a few mV. For this reason, working in weak inversion is still acceptable.

The transconductance of a MOS transistor biased in weak inversion is given by [4.8]:

$$g_{m-WI} = \frac{I_d}{nV_T} \tag{4.93}$$

where I_d is the drain current, $V_T = kT/q = 26$ mV and n, usually referred to as "slope factor", is 1.4-1.5 for bulk CMOS processes and 1.2-1.3 for SOI processes.
If devices M_{o1} and M_{o2} work in strong inversion region and are saturated, we obtain:

$$A_1 = \frac{g_{mi}}{g_{mo}} = \frac{I_{d1}\left(V_{GS} - V_{TH}\right)_0}{2I_{do}nV_T} \tag{4.94}$$

where $I_{d1} = I_{tail}/2$ is the drain current of M_1-M_4, $\left(V_{GS} - V_{TH}\right)_0$ is the overdrive voltage of M_{o1}-M_{o2} and $I_{do} = I_o/2$ is their drain current. It should be noted that the differential output current flowing into the load should be always decisively lower than I_0, to avoid non-linear behaviour. Moreover, saturation of M_{21} has to be guaranteed and the following equation holds:

$$\left(V_{GS} - V_{TH}\right)_0 \leq V_{CMout} - \left(V_{GS} - V_{TH}\right)_{21} - V_{THn} \tag{4.95}$$

where V_{CMout} is the output common mode of the preamplifier. These considerations have been taken into account to properly size the devices.
The input noise PSD of the preamplifier can be calculated considering the noise contributions of relevant devices. In this circuit, the transistors that significantly contribute to the input noise are M_1-M_2 and M_3-M_4 (input differential pairs) and M_{11}-M_{13} (biasing devices). Then, preamplifier input noise PSD is given by:

$$S_{v-pre} = 4S_{vi} + \frac{2S_{I11}}{g_{mi}^2} \tag{4.96}$$

where S_{vi} is the input voltage noise PSD of M_1-M_4 and S_{I11} is the current noise PSD of M_{11} and M_{13}. The thermal component of the PSD S_{vi-th} can be calculated considering that the pairs work in sub-threshold region. The drain current noise PSD of a MOS transistor biased in this condition is given by:

$$S_{I-wi} = 2qI_d \tag{4.97}$$

where q is the electron charge and I_d is the drain current. Therefore:

$$S_{vi-th} = \frac{S_{I_w i}}{g_{mi}^2} = \frac{2qI_d n^2 V_T^2}{I_d^2} = 2n^2 kT\frac{V_T}{I_d} \tag{4.98}$$

On the other hand, the thermal noise component of S_{I11} is given by:

$$S_{I11-th} = \frac{8}{3}kTg_{m11} \tag{4.99}$$

since they are saturated and in strong inversion condition. Therefore, the thermal component of S_{v-pre} becomes:

$$S_{v-pre-th} = 16n^2kT\frac{V_T}{I_{tail}} + \frac{128}{3}kT\frac{I_b}{(V_{GS}-V_{TH})_{11}}\frac{4n^2V_T^2}{I_{tail}^2} \tag{4.100}$$

It is clear that increasing I_{tail} while biasing the input pairs in weak inversion region helps to decrease the thermal noise PSD.
On the other hand, the flicker noise component should be evaluated at 20 kHz, since chopper modulation is applied. The flicker component of the pairs input noise PSD is given by:

$$S_{vi-fl}(f) = \frac{N_{FN}}{W_1L_1}\frac{1}{f} \tag{4.101}$$

while the flicker component of M_{11}-M_{13} current noise PSD is given by:

$$S_{I11-fl} = \frac{N_{FP}}{W_{11}L_{11}}\frac{g_{m11}^2}{f} \tag{4.102}$$

Therefore, $S_{v-pre-fl}$ at 20 kHz results to be:

$$S_{v-pre-fl}(f_{ch}) = 4\frac{N_{FN}}{W_1L_1}\frac{1}{f_{ch}} + 2\frac{N_{FP}}{W_{11}L_{11}}\frac{g_{m11}^2}{g_{mi}^2} \tag{4.103}$$

From this equation, it can be observed that increasing gate area helps to reduce flicker noise as usual. Since at the same time working in weak inversion is necessary, this can be preferably achieved increasing W rather than L. Moreover, flicker and thermal noise can be minimized keeping g_{m11} as smaller than g_{mi} as possible. This can be achieved increasing the overdrive of M_{11} and M_{13}. However, this is possible only up to a certain point without decreasing robustness of the biasing against process corners and temperature variations. In addition, increasing the gate area of M_{11} and M_{13} increases in turn their C_{gs} degrading the common-mode feedback loop stability, since the non-dominant pole of the loop is moved to lower frequencies. Therefore, the noise contribution of M_{11} and M_{13} cannot be made negligible as it should be.
The preamplifier sizing has been operated trying to optimize the noise level, power consumption and silicon area [4.3]. The tail current I_{tail}=42.5 µA is obtained by means of an high swing current mirror from a reference current I_{bias}=4.25 µA. The load bias current I_o has been set to 940 nA. The bias

voltages are:

$$V_{b0} = 0.87\text{V}$$
$$V_{b2} = 2.03\text{V} \tag{4.104}$$

The preamplifier sizing is reported in Tab. 4.3. With this sizing, $(V_{GS} - V_{TH})_1 =$

MOSFET	W	L	M
M_{1-4}	60	2	100
M_{5-8}	4	6.5	200
$M_{9,10}$	20	1	10
$M_{11,14}$	5	5	20
$M_{12,13}$	2.5	40	1
M_{15}	8	1	2
$M_{16,17}$	8	1	2
M_{18}	12	1	2
$M_{19,20}$	12	1	20
M_{21}	5.5	1	1
$M_{b1,b2}$	1	47	1
$M_{o1,o2}$	1	105	1

Table 4.3: Preamplifier sizing.

-188 mV.

The preamplifier gain, characterized by means of AC simulations, is 616.6, corresponding to 55.8 dB, and is flat up to 68 kHz. The bandwidth is limited by the dominant pole associated with output resistance and capacitance. The second pole is significantly higher than the GBW product.

The input noise PSD is -156.24 dB at 20 kHz(15.4 nV/$\sqrt{\text{Hz}}$). The differential pairs devices contribute each with 6.2 nV/$\sqrt{\text{Hz}}$, while $M_{11,13}$ with 6.5 nV/$\sqrt{\text{Hz}}$. The former contribution is dominated by thermal noise, while the latter by flicker noise.

The output common-mode has been set to 1.925 V. The common-mode loop has a GBW of 2.2 MHz and a non-compensated phase margin of 25°. In order to ensure stability, two load capacitors of 5 pF have been added. In these conditions, the phase margin increases up to 45°. On the other hand, the bandwidth of the preamplifier decreases to around 20 kHz. This causes a gain decrease to the chopper modulation, since the clock harmonics fall over the pole. This

effect can be counteracted by properly choosing the integrating capacitance value, in order to compensate for the gain decrease, if necessary.

4.4.4 G_{m3} design

The voltage-to-current conversion necessary to implement INT1 is operated by the transconductor G_{m3}. Its output current is then integrated by the capacitances C_1. Once the filter cut-off frequency f_c and the quality factor Q have been fixed, the integrating constant is given by Eq. 4.87. Due to preamplification, the ratio g_{m3}/C_1 results to be small. For the given $A_1 = 616.6$, we obtain:

$$\frac{g_{m3}}{C_1} = \frac{\omega_{01}}{2A_1} \approx 144 \ \text{rad/s} \tag{4.105}$$

This small unity-gain frequency should be achieved increasing the channel length of M_1 and M_2 rather than C_1 for better area efficiency. This topic will be deeply investigated in Chap. 6.

The transconductor G_{m3} is based on a p-type pseudo-differential pair working in saturation region to achieve a smaller transconductance with respect to NMOS. The pseudo-differential pair allows linear operation with low input noise. The working principle of this simple circuit will be presented later in Chap. 6. A drawback inherent to this configuration is the dependency of the transconductance on the input common-mode. However, this voltage is fixed by the CMFB circuit of the preamplifier. Tuning has not been provided since g_{m3} mainly impacts bandwidth, which is not a critical specification in the target application. The schematic is shown in Fig. 4.12. The folded-cascode configura-

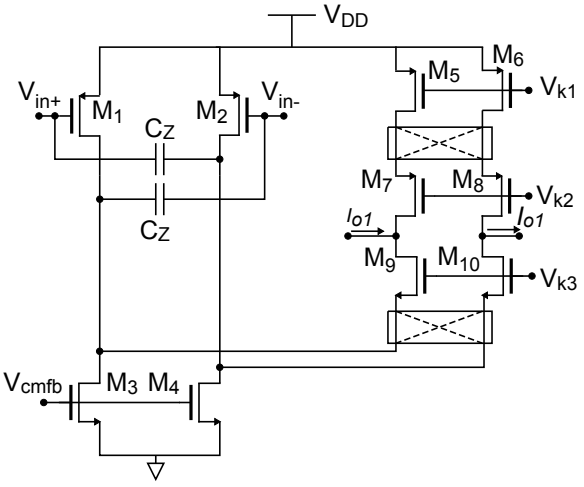

Figure 4.12: Schematic of G_{m3} transconductor.

tion guarantees a wide output swing and an high output resistance. The modulators implement chopper modulation and are positioned at low impedance nodes, in order not to degrade the voltage gain of the transconductor. The lower one demodulates signal and modulates preamplifier and G_{m3} offset and noise, while the upper one modulates offset and noise coming from the biasing devices M_5 and M_6. The common-mode feedback circuit driving the gates of M_3 and M_4 is not shown.
The transconductance g_{m3}, intended as the ratio between the output current I_{o1} and the input differential voltage of the integrator v_{in}, is given by:

$$g_{m3} = \frac{I_{o1}}{v_{in}} = \frac{g_{m1-3}}{2} \tag{4.106}$$

where g_{m1-3} is the transconductance of M_1 and M_2. In order to minimize the area consumption, taking at the same time into account noise and feasibility, we have chosen:

$$g_{m1-3} = 33 \text{ nS} \tag{4.107}$$

This value has been achieved by sizing M_1 and M_2 with $W = 0.8$ µm and $L = 400$ µm. Unfortunately, with such a low transconductance the singularities of g_{m3} are shifted to frequencies near f_{ch}. In particular, the right half plane zero introduced by the gate-drain capacitances of M_1 and M_2 degrades the phase response of the transconductor. This zero is found at:

$$s_{z1} = \frac{g_{m1-3}}{C_{dg1-3}} \tag{4.108}$$

where C_{dg1-3} is the gate-drain capacitance of M_1 and M_2. Due to the extremely long channel, C_{dg1-3} is around 350 fF (as shown by simulations). This means that the zero frequency f_{z1} is around 15 kHz. This reflects into a reduction of the effective transconductance of near 60% when chopper is applied, as measured with transient simulations. In principle this effect helps to lower the transconductance, but its unreliability due to process and temperature variation sensitivity suggests to avoid its exploitation. The capacitances C_z compensate this degradation introducing a feedforward signal path, as clarified in Fig. 4.13, which shows the amplitude and phase response of g_{m3}. Transient simulations have shown that by choosing C_z equal to 350 fF, the degradation of g_{m3} is almost perfectly recovered. Subsequent tests have shown the robustness of this technique also when corners and temperature are swept.
The devices contributing to G_{m3} input noise PSD are M_1-M_6. When thermal

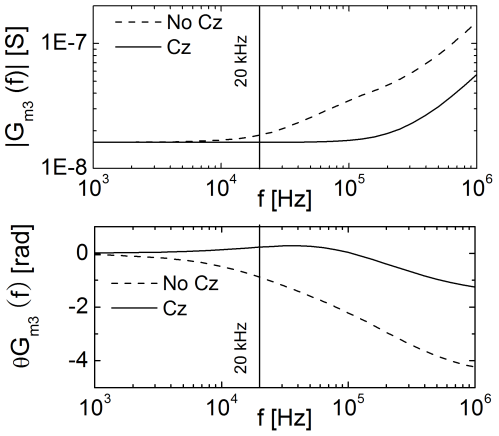

Figure 4.13: Frequency response of g_{m3}.

noise is concerned, the input noise PSD $S_{v-Gm3-th}$ is given by:

$$S_{v-Gm3-th} = \frac{16}{3}\frac{kT}{g_{m1-3}}\left[1 + \frac{I_{d3}\left|V_{GS}-V_{TH}\right|_1}{I_{d1}\left(V_{GS}-V_{TH}\right)_3} + \frac{I_{d5}\left|V_{GS}-V_{TH}\right|_1}{I_{d1}\left|V_{GS}-V_{TH}\right|_5}\right] \quad (4.109)$$

where I_{d1}, I_{d3} and I_{d5} are the drain currents of M_1, M_3 and M_5, respectively. On the other hand, the flicker noise component is given by:

$$\begin{aligned} S_{v-Gm3-fl}\left(f\right) = \frac{2}{f}\left[\frac{N_{FP}}{W_1L_1} + \frac{N_{FN}}{W_3L_3}\left(\frac{I_3\left|V_{GS}-V_{TH}\right|_1}{I_1\left(V_{GS}-V_{TH}\right)_3}\right)^2\right. \\ \left. + \frac{N_{FP}}{W_5L_5}\left(\frac{I_5\left|V_{GS}-V_{TH}\right|_1}{I_1\left|V_{GS}-V_{TH}\right|_5}\right)^2\right] \end{aligned} \quad (4.110)$$

It is clear that having a low transconductance due to the filter specifications badly impacts the noise performances of the integrator. The preamplifier helps to mitigate this effect. The transconductor sizing has been operated looking for an optimum trade-off between total noise at the preamplifier input, capacitance area and layout feasibility. The drain currents have been chosen as follows:

$$I_{d1} = 12 \text{ nA} \quad (4.111)$$

$$I_{d3} = 36.5 \text{ nA} \quad (4.112)$$

$$I_{d5} = 24.5 \text{ nA} \quad (4.113)$$

The overdrive voltage of the input pair has been fixed to 0.72 V, while the overdrive of M_3, M_4 has been fixed to 0.3 V. Biasing devices M_5 and M_6 have an overdrive of 0.42 V. This sizing is not optimal for noise, since the overdrive of M_1 and M_2 is larger than the others. This choice was mainly due to swing

and robustness considerations. The biasing voltages of G_{m3} are:

$$V_{k1} = 2.2 \text{ V} \tag{4.114}$$

$$V_{k2} = 1.8 \text{ V} \tag{4.115}$$

$$V_{k3} = 1.36 \text{ V} \tag{4.116}$$

The transconductor sizing is reported in Tab. 4.4. The modulators have been

MOSFET	W	L	M
$M_{1,2}$	0.8	400	1
$M_{3,4}$	2	380	1
$M_{5,6}$	2	250	1
$M_{7,8}$	6	18	1
$M_{9,10}$	4	85	1

Table 4.4: Transconductor G_{m3} sizing.

implemented as simple pass-gate switches.
With this sizing, G_{m3} noise PSD at 20 kHz results to be -107.6 dB. At the input of the preamplifier noise PSD at 20 kHz is -155.5 dB (16.7 nV/$\sqrt{\text{Hz}}$). From Eq. 4.105 it is possible to obtain C_1, which results to be 115 pF. However, since chopper modulation impacts the actual transconductance of the first integrator, as it can be easily observed with simulations, C_1 has been decreased to 88 pF, in order to fit the ideal Butterworth filter response.

4.4.5 INT2 design

The second integrator has been designed with a g_m – OPAMP topology, in order to properly drive the resistive feedback network. Its topology is shown in Fig. 4.14. The differential pairs M_1-M_2 and M_3-M_4 implements the function of G_{m4a} and G_{m4b} (see Fig. 4.8). The operational amplifier is a single-stage OTA constituted by M_{14}-M_{17}. The Miller capacitances C_2 implement the integrating function. With the chosen topology, the output can have a rail-to-rail swing. The differential output voltage V_{out} in the Laplace domain can be calculated:

$$V_{out}(s) = \frac{g_{m1-4}}{2} \frac{v_a - v_b}{C_2 s} \tag{4.117}$$

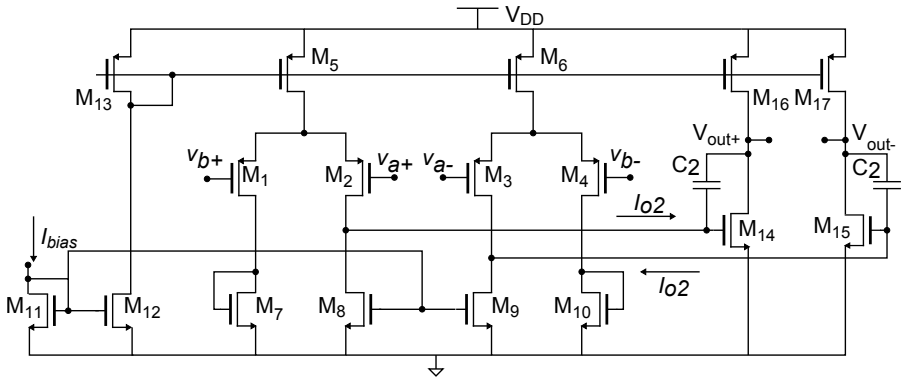

Figure 4.14: Schematic of the second integrator.

where g_{m1-4} is the transconductance of M_1-M_4 and $v_a = v_{a+} - v_{a-}$ and $v_b = v_{b+} - v_{b-}$. Considering that $v_a = V_{int1}$, we obtain:

$$V_{out}(s) = \frac{g_{m1-4}}{2} \frac{V_{int1} - V_{out}}{C_2 s} \tag{4.118}$$

Thus, it can be observed from Eq. 4.66 that $g_{m4} = g_{m1-4}/4$. The value of the transconductance has been set taking into account Eq. 4.67 and the design specifications (see Eq. 4.87.

The described topology performs also amplification of the common mode input voltage, since it is not cancelled by the input pairs. Defining V_{Ca} as the CM voltage at the port A, and feeding back the output to port B, it can be written:

$$V_{CMO}(s) = \frac{V_{Ca}}{1 + 2\frac{C_2}{g_{m1-4}s}} \tag{4.119}$$

The output CM voltage V_{CMO} results to be fixed to V_{Ca}, which is fixed to the output CM of the first integrator (1.41 V).

As described before, the input noise PSD of INT2 is processed by the pass-band function $H_{BP}(s)$, which as a unit value at f_c. Therefore, the main contribution of this block to the overall noise will be found around this frequency. The devices contributing to input noise PSD are M_1-M_4, M_5-M_6, M_8-M_9 and M_{14}-M_{17}. The latter contribution can become relevant because the gain of the differential pairs is limited due to the low g_{m1-4} value. Further calculations are omitted, as they are very similar to previous blocks. Same considerations hold also for noise optimization.

The sizing has been operated trying to obtain optimum trade-offs between noise

and area. The input transconductance g_{m1-4} has been set:

$$g_{m1-4} = 378 \text{ nA} \tag{4.120}$$

The differential pair bias current is 350 nA. The output branches are biased with 20 µA, in order to decrease the output resistance and to properly drive the feedback network. The devices sizing is shown in Tab 4.5. With this sizing,

MOSFET	W	L	M
M_{1-4}	2	130	2
$M_{5,6,13}$	30	85	1
M_{7-10}	1.2	300	1
$M_{11,12}$	1.2	300	2
$M_{14,15}$	6	6	1
$M_{16,17}$	120	2	1

Table 4.5: Transconductor G_{m4} and INT2 sizing.

we also have $(V_{GS} - V_{TH})_{14} = 105$ mV and $(V_{GS} - V_{TH})_{16} = 600$ mV. The output resistance is around 2 MΩ, well above the load resistance given by the feedback network (400 kΩ).
The output noise at 200 Hz is -118.8 dB. This contribution can be referred to the amplifier input divided by the gain (around 46 dB). Therefore its contribution to the input noise is -164.8 dB at 200 Hz and is therefore negligible. However, the main noise contributors are M_5, M_6, M_8 and M_9, while the input pairs contribution is negligible.
Finally, capacitance C_2 have been set to 107 pF to satisfy Eq. 4.87.

4.4.6 OA-CM design

The operational amplifier necessary to implement the input common-mode equalization is shown in Fig. 4.15. The circuit amplifies the difference between the input common-mode voltages. The first stage consists in the input pairs M_1-M_2 and M_3-M_4, loaded by the current mirror M_5-M_6. The class AB output stage, adopted to save current, since the amplifier has to sink and source current only when input and output common-mode voltages of the instrumentation amplifier are different, consists in the level shifter M_{12}-M_{15} and the amplifying stage M_{13}-M_{14}. The Miller compensation is achieved by means of the capacitance C and the zero-nulling resistor R.

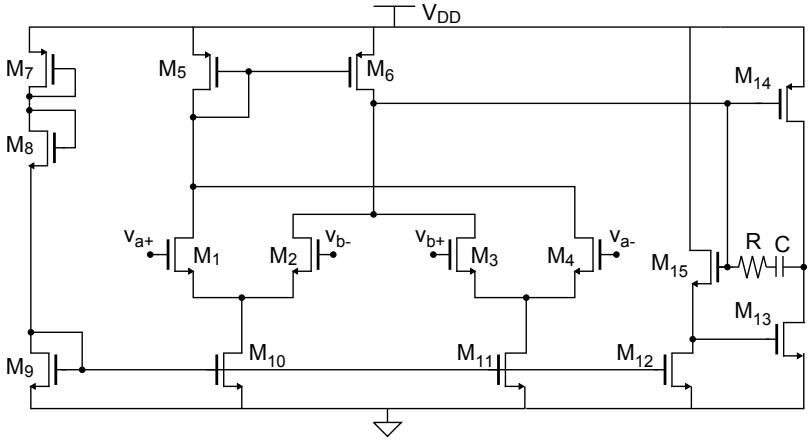

Figure 4.15: Schematic of OA-CM.

The gain of OA-CM is given by:

$$A_{OA-CM} = 2g_{m1-CM}r_{o1}\left(g_{m13-CM} + g_{m14-CM}\right)r_{o2} \tag{4.121}$$

where g_{m1-CM}, g_{m13-CM} and g_{m14_CM} are the transcondutances of M_1-M_4, M_{13} and M_{14}, respectively, while r_{o1} and r_{o2} are the output resistances of the first and second stages.

Noise performances of this block are not important, since it only acts on the common-mode and has no effect on the differential noise at the input of the amplifier. The op-amp OA-CM has then been sized trying only to keep offset in the mV level with a low power consumption. Moreover, no particularly large bandwidth is required, since input and output common-modes are not expected to vary during normal working of the amplifier. The sizing is reported in Tab. 4.6. The capacitance C is 13 pF and the nulling resistor $R = 15$ kΩ.

MOSFET	W	L	M
M_{1-4}	5	24	4
$M_{5,6}$	8	9	5
M_7	8	9	1
$M_{8,15}$	0.6	40	1
$M_{9,12}$	1.3	5	1
$M_{10,11}$	1.3	5	5
M_{13}	1.3	5	30
M_{14}	8	9	39

Table 4.6: Sizing of CM operational amplifier.

With this sizing, the GBW results to be 325 kHz, the phase margin larger than 68° and the input offset lower than 1 mV (evaluated by means of several Monte-Carlo runs). The stability of the common-mode loop will be described later. However, it is not a big concern: although OA-CM has to drive the input capacitances of the instrumentation amplifier (around 15 pF), the feedback resistors $R_1/2$ act as decoupling resistors adding a zero and helping to increase the phase margin.

4.4.7 Modulator SA-FB design

The modulator SA-FB, positioned before the feedback network, has been implemented with pass-gate switches. In this way, even when the output is fully swinging, the on-resistance of the switch remains low. However, due to the dependence of the on-resistance of the pass-gate switch on the source voltage, through the equation:

$$r_{on} = \frac{1}{\beta(V_{GS} - V_{TH})} \tag{4.122}$$

they can introduce distortion and degrade the linearity of the amplifier. The switches have then been sized in order to minimize their r_{on}. Actually, they are in series with R_2, which is 200 kΩ. Therefore, their effect on the amplifier linearity will be low, since the on-resistance of the switches influences only marginally the gain. The P and N switches have been sized with $W = 5$ µm and $L = 0.35$ nm. The on-resistance is 720 Ω. The gain A_0 results then to be given by:

$$A_0 = \frac{R_1 + 2\,(R_2 + r_{on})}{R_1} \approx 201.72 \tag{4.123}$$

The on-resistance couldn't be further reduced: an increase of the width corresponds to a switch capacitance increase. This, in turn, leads to an increase of the output spikes super-imposed to the signal. This will be clarified later, in the simulation section.

4.5 Simulations and characterization

The circuit design and sizing phase has been supported by an extensive use of the electrical simulator. After this design step, the designed instrumentation amplifier has been thoroughly characterized before starting to carry out the layout. Functionality and effectiveness of the described approaches have been analyzed.

The simulations have been performed with the ELDO (Mentor Graphics) sim-

ulator, using the BCD6s process device models (MOS MODEL 9) [4.9]. Unless differently specified, in all the following simulations the input common-mode has been set to 1.41 V (output CM voltage).
Initially, stability of the feedback loops has been checked. The input common-mode stabilizing loop has a phase margin of 80° for a GBW of 300 kHz. The GBW of the loop coincides with the GBW of the op-amp since the latter practically acts as a unit gain buffer. On the other hand, the phase margin of the overall differential feedback loop is 60° for a loop GBW of 200 Hz. The high feedback factor (1/201) helps in easily achieving stability, though two integrator stages are found in the signal path.
Fig. 4.16 shows the output voltage when an input step of 1 mV is applied. The output voltage V_{out} settles to the desired value with a transient closely matching the Butterworth response. The inset shows a magnified view of the

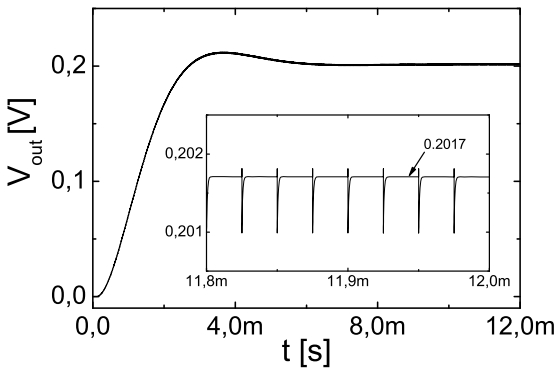

Figure 4.16: Transient response of the amplifier when a 1 mV step is applied.

waveform between 11.8 and 12 ms. The average gain results to be equal to around 201.7, as expected from calculations. The spikes are mainly due to the position of the SA-FB modulator. Actually, when chopping occurs, the sign inversion on the feedback port is delayed with respect to the sign inversion on the signal port. For this reason, for a short time the signal and feedback voltage have same sign. This phenomenon translates into the output spikes. The delay is mainly given by the time constant formed by the input capacitance C_{in} of the amplifier, estimated around 15 pF, and $R_{eq} = R_1//2R_2 \approx R_1$, which is $R_{eq}C_{in} = 0.15$ µs. Positioning the switch at the preamplifier input would decisively reduce the output spikes amplitude, but would impact gain accuracy in a not negligible and unacceptable way, as previously clarified. However, the energy associated with these spikes is low, and does not significantly changes the average value of the gain.

The input/output characteristic of the amplifier is shown in Fig. 4.17. The

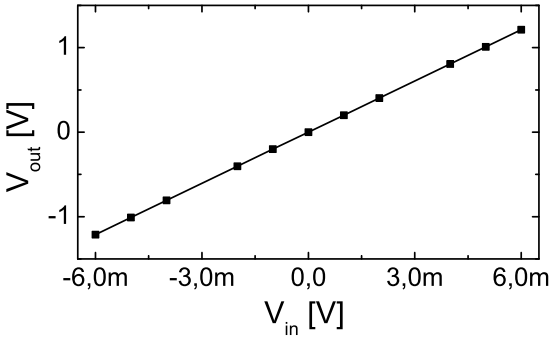

Figure 4.17: Input/output characteristic of the instrumentation amplifier.

range within which the maximum deviation from the ideal characteristic is 0.1% is extended from -6 to 6 mV. The small linear range is due to the sub-threshold biasing of the input differential pairs. However, since the target sensor output amplitude is small ($\approx$ 1 mV), the linear range can be considered sufficiently wide.

Due to the modulated nature of the chopper amplifier, steady-state simulations such as .SSTAC and .SSTNOISE have been used to calculate the frequency response and output noise of the amplifier. Fig. 4.18 shows the amplitude and phase response of the amplifier. The -3 dB bandwidth is 195.5 Hz; at this

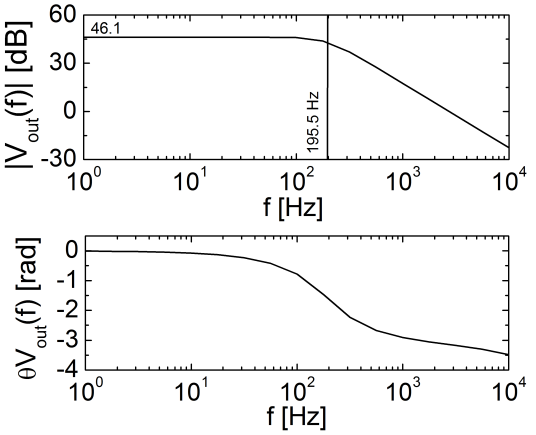

Figure 4.18: Amplitude and phase response of the amplifier as obtained from SSTAC simulations.

frequency the gain attenuation is -3 dB, and above the roll-off is -40 dB/dec, as usual in case of Butterworth filters. The output noise is shown in Fig. 4.19. The noise PSD has been calculated taking into account 100 harmonics of f_{ch},

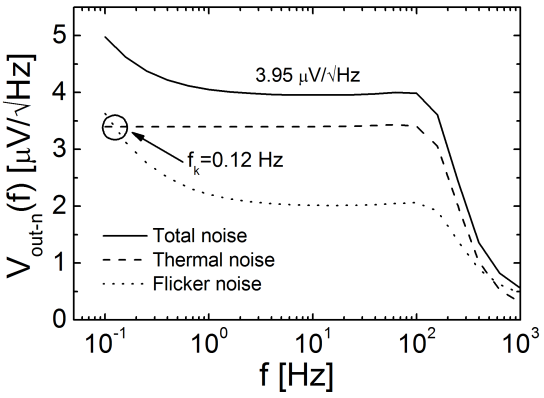

Figure 4.19: Output noise PSD of the instrumentation amplifier obtained by means of SSTNOISE simulations.

to properly consider the thermal noise fold-over related to chopper modulation. The corner frequency f_k results to be equal to 0.12 Hz. The residual flicker noise at very low frequencies is mainly due to the common-gate devices of the cascode stages. Although very small, their flicker noise contribution becomes relevant at these frequencies [4.10]. The output noise density of 3.95 $\mu V/\sqrt{Hz}$ simulated in the flat region corresponds to a 19.6 $nV/\sqrt{Hz}$ input noise density. Integrating the input noise PSD between 0.1 Hz and 200 Hz an *rms* input noise voltage of around 300 nV is obtained. Considering the amplifier total current consumption, which is around 170 µA, the Noise Efficiency Factor [4.11] can be calculated.

$$NEF = v_{in,rms}\sqrt{\frac{2I_{sup}}{\pi V_T 4kTB}} \tag{4.124}$$

where $v_{in,rms}$ is the input *rms* noise voltage, I_{sup} is the supply current and B is the amplifier bandwidth, considered in this case 200 Hz. The obtained NEF is 10.6. The values is slightly larger than the best reported in the literature ([4.10], [4.5], [4.12]), but is still respectable. The input dynamic range can also be calculated:

$$DR = \frac{max - signal}{min - signal} = \frac{max - signal}{v_{in,pp}} \tag{4.125}$$

where $max-signal$ is the maximum signal that the amplifier can process within a given linearity range and $v_{in,pp}$ is the peak-to-peak input noise voltage. Considering a maximum signal of 6 mV and a crest factor of 2, the obtained DR is 74 dB (slightly lower than 12 bits).

The amplifier DC resolution is limited by the offset voltage. Chopper modulation has been employed to drastically reduce its impact. However, due to the

factor described in the first chapters, a residual DC offset is still present. It has been estimated by means of several MonteCarlo runs. The histogram depicted in Fig. 4.20 represents the input offset distribution obtained from 50 MonteCarlo runs. The offset standard deviation results to be lower than 1 µV (800

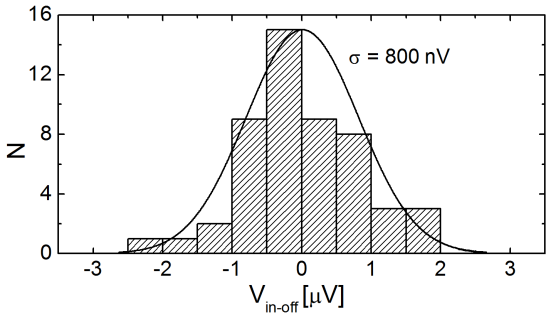

Figure 4.20: Input offset distribution as obtained from 50 MonteCarlo runs.

nV). This kind of results are usually not completely affordable, since the phenomena from which residual offset is originated, e.g. charge injection mismatch, is not enough accurately predicted by the electrical simulators. However, this quantity represents an initial estimation to be refined by further measurements on the fabricated chip. In all the MonteCarlo runs the output offset ripple amplitude has been measured and resulted to be lower than 10 µV in all cases (some of them are shown in Fig. 4.21) confirming the efficiency of the approach in filtering the offset ripple. Gain accuracy has also been estimated by means

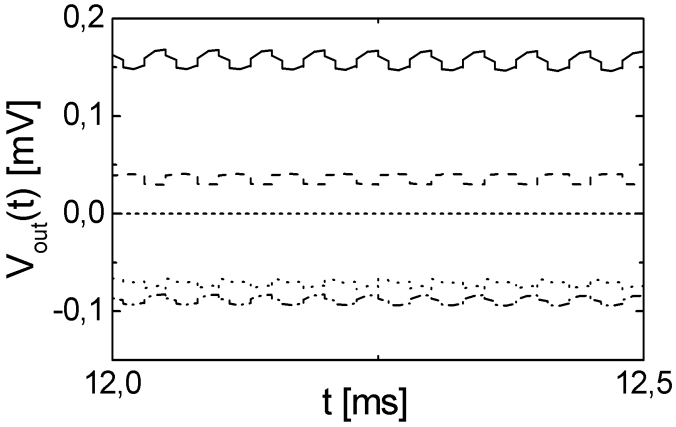

Figure 4.21: Worst-cases output offset ripple.

of MonteCarlo simulations. The gain error has been defined as:

$$\epsilon_g = \frac{A_0 - A_{0sim}}{A_0} \tag{4.126}$$

The resulting distribution is reported in Fig. 4.22. The standard deviation of

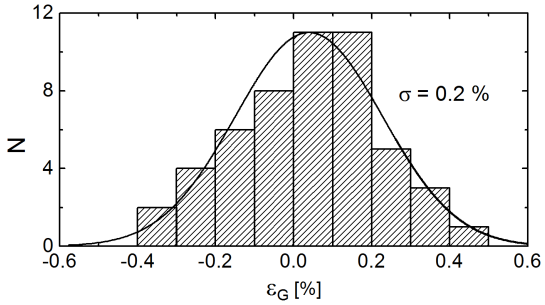

Figure 4.22: Gain error distribution as obtained from 50 MonteCarlo runs.

ϵ_g results to be equal to 0.2%. This is mainly due to the resistive feedback network. Actually, *ad hoc* MonteCarlo simulations performed on this network have shown that the feedback factor spread due to mismatch is around 0.2%. The latter can be decreased investing more silicon area into the feedback network, when necessary.

Gain precision has been tested also versus input common-mode variations, in order to test the effectiveness of the common-mode loop. To do so, unbalanced source resistances of 51 and 49 kΩ, respectively, have been added in series with the non-inverting and inverting input terminals. Then, the gain has been evaluated at different CM voltages, with the output CM voltage fixed at 1.41 V. The gain error has been tabulated in Tab. 4.7. A one order of magnitude improvement can be observed with respect to the calculations performed above, when no CM correction was present.

V_{CM}	ϵ_g
0.8	0.13%
1.2	0.08%
1.7	-0.06%
2.2	0.17%

Table 4.7: Gain error introduced by CM mismatch.

Since input bias and offset currents are particularly detrimental in case of high series resistance input sources, several MonteCarlo runs have been performed to try to estimate their amount. In a chopper amplifier, input bias and offset currents are mainly due to charge injection [4.6]. The simulations have shown a bias current around 115 pA, while MonteCarlo runs highlighted an average offset current of 200 fA, with a standard deviation around 45 pA. Also in this case the simulated quantities are not fully reliable, due to the poor modelling

of charge injection. However, the very small value returned by simulation highlighted that no current is sinked by the amplifier as a result of chopping and indirectly confirms the efficiency of the port-swapping technique in increasing the input impedance.
Another test performed in this direction consisted in sweeping the total input series resistance in a balanced configuration. The total resistance has been swept from 100 kΩ to 1 MΩ. The resulting gain trend is shown in Fig. 4.23. Contrarily to what expected, the gain tends to increase for higher series resis-

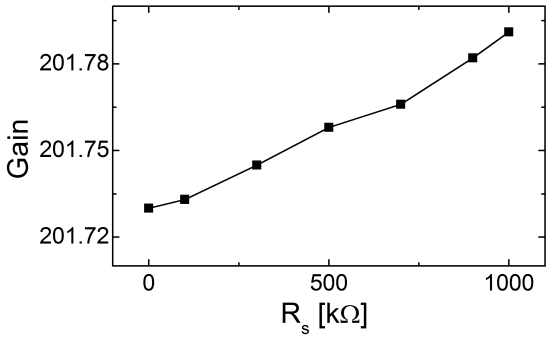

Figure 4.23: Gain trend when input resistance is swept.

tances, passing from 201.73 to 201.79 (0.08%). This can be explained making once again reference to offset currents related to charge injection. By applying an input differential voltage, a small mismatch of the switch electrical conditions is introduced. Then, the small offset current originated introduces the gain error. Also this simulation indirectly confirms the efficiency of the proposed technique in increasing the input impedance of the instrumentation amplifier. However, due to the dominance of the offset currents, it is hard to exactly quantify the current sinked by the instrumentation amplifier.
Finally, reliability simulations have been performed. The transient output voltage when a 1 mV step is applied and slow corners at 80° C or fast corners at 0° have are selected is shown in Fig. 4.24. It should be noted that the transient responses are different over the different corners. This is due to the variation of ω_c and Q associated with the variation of the transconductance of the integrators. However, this is not a big problem in this kind of applications, where a very accurate bandwidth is not important. In case a precise ω_c is required, g_m tuning has to be provided. On the other hand, gain precision is not particularly influenced by the process, since a variation of 0.04% has been obtained from slow to fast corner, and a gain variation of 0.06% has been observed when temperature is swept from 0°to 80° C.

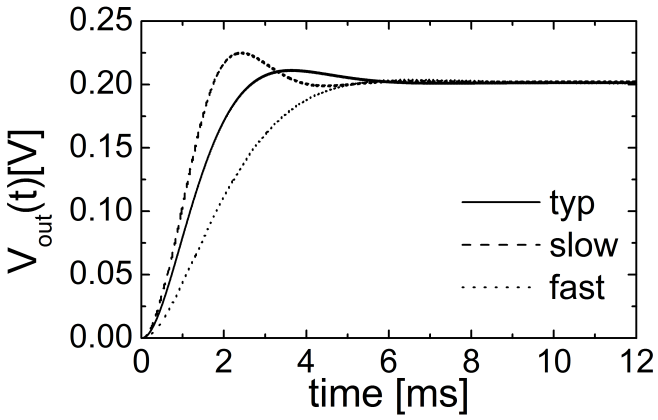

Figure 4.24: Transient response when slow, typical or fast corners are selected.

4.6 Conclusions

In this chapter an instrumentation amplifier architecture based on current-feedback principle has been presented. The amplifier is targeted to interface MEMS flow sensors, and is therefore characterized by low offset and low noise. Chopper modulation has been used to meet these specifications and a port-swapping technique has been implemented to increase the gain accuracy and the input impedance of the amplifier. The offset ripple is intrinsically filtered thanks to the presence of two G_mC integrators in the signal path.
A prototype has been designed with devices of a commercial CMOS process (BCD6s from STMicroelectronics). The bandwidth has been limited to 200 Hz with a quality factor $Q = 200$. The input noise is lower than 20 nV/$\sqrt{\text{Hz}}$, with a current consumption of 170 µA, leading to a NEF of around 10.6. The proposed approach made the amplifier very robust to large input common-mode variations, on a 0.8-2.2 V range. The gain accuracy, improved by means of dynamic element matching, is characterized by a 0.2% standard deviation.
The reported characteristics make the amplifier a valid alternative to other solutions in the literature, thanks to its high performances obtained with a compact architecture.

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Chapter 5

Smart chip design and layout

The proposed interface has been integrated into a complete System-on-Chip for gas flow measurement. The chip includes the instrumentation amplifier, three flow sensors, a programmable current mirror for sensor offset compensation, a current reference, a relaxation oscillator for chopper clock generation and some analog multiplexers. In this chapter some details about the design and the layout of the smart chip will be reported.

5.1 Programmable current mirror design

As described in Chap. 1, the intrinsic sensor offset due to unavoidable mismatch of the sensing structures can be compensated driving the heaters with an unbalanced current. To this purpose, a programmable current source, capable of driving the heaters with a programmable 10-bit differential current, has been implemented.
The reference current has been obtained by a standard voltage regulator, shown in Fig. 5.1. The operational amplifier, thanks to negative feedback, sets V_{ref} at node H. Therefore, the current I_{ref} results to be given by:

$$I_{ref} = \frac{V_{ref}}{R_1} - \frac{V_{DD} - V_{ref}}{R_2} \tag{5.1}$$

The cascode transistor M_2 decisively increases the output resistance of the mirror branches. The importance of this feature will be explained later. The resistor R_2 has been added to enable switching off the reference current with a

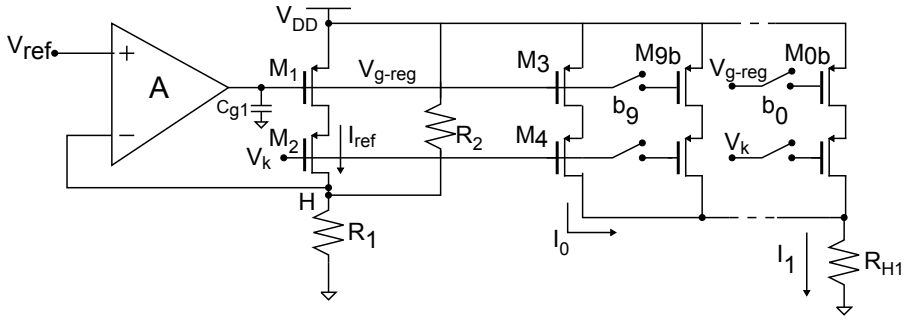

Figure 5.1: Voltage regulator and programmable current mirror.

non-zero V_{ref}. It can be shown that, with $R_2 = 5R_1$, I_{ref} is nullified when:

$$V_{ref}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)=\frac{V_{dd}}{R_2} \tag{5.2}$$

This solution has been chosen because to nullify I_{ref}, V_{ref} should reach 0 V. This would imply the use of a p-type input pair, which cannot swing up towards the supply rail. Therefore, to cover the whole necessary input range, a double-pair OTA should be used. To simplify the design, single n-type input pair has been used and this solution has been instead adopted.

The regulated current I_{ref} is then mirrored by a programmable current mirror, configured by a 10 bit word (b_9-b_0). A fixed component, I_0, is always on, while a programmable component is defined by M_{9b}-M_{0b}, which are binary-weighted through their multiplicity. This means that M_3 and M_{9b-0b} are scaled replicas of M_1, which, in turn, is a scaled replica of an elementary transistor, whose size has been chosen in order to optimize overall noise and linearity versus silicon area. The obtained total current is then delivered to the heater, here represented by R_{h1}. If the current delivered to the heater changes, the voltage drop on it will vary. Therefore, if no cascode devices are added, the V_{ds} variation of M_{9b}-M_{0b} will introduce an additional modulation of the current, adding an integral non-linearity to the input-output characteristic of the programmable current source [5.1]. This consideration sets a lower limit to the current mirror branches output impedance Z_{out}.

An identical replica of the configurable section of the current mirror is used to drive the second heater R_{h2}. The switches of this section are driven by the inverted word $\overline{b_9}$-$\overline{b_0}$. Defining I_2 as the current flowing into the heater R_{h2}, by choosing the configuration word it is possible to configure the differential current $I_1 - I_2$ flowing through the heaters.

The fixed term, I_0, is the same for both the branches, and has been chosen

equal to 800 µA. The configurable part delivers a maximum current of 409.6 µA, with a resolution of 10 bit. With this choice, the output differential span is ±409.6 µA. This means that the LSB current is 400 nA. The nominal value of the current flowing through each heater is 1.0048 mA. The reference current has been chosen equal to 128 LSB, i.e. 51.2 µA. This value of I_{ref} has been chosen in order to optimize the common-mode and differential current noise associated with the output current of the mirror. It can be easily shown that choosing I_{ref} in the order of a few LSB, thus implying the use of higher current mirror ratios, degrades the noise performances. This LSB is obtained by choosing $V_{ref} = 2.2$ V, since $R_1 = 40$ kΩ and $R_2 = 200$ kΩ. On the other hand, the current is switched off when V_{ref} is lower than 0.55 V.
The size of the elementary transistor (M_{0b}), associated with the LSB current, has been chosen making reference to the target differential non-linearity. To obtain a monotonic input-output DAC characteristic it is necessary to guarantee that the DNL is lower than 0.5 LSB for each code transition. A good estimation for the worst case DNL for this kind of circuit, very similar to a current steering DAC [5.1], can be obtained considering the transition from the code 0111111111 to 1000000000, where the largest number of current sources is switched from on to off state and vice versa. In this case, the maximum amount of error current due to mismatch is injected into the output current, causing a possible error greater than 0.5 LSB. The standard deviation of this transition affecting each of the two current mirrors can be written:

$$\sigma_{\Delta I^2} = \sigma^2 \left[2^{N-1} I_{LSB} - \left(2^{N-1} - 1\right) I_{LSB}\right] = \tag{5.3}$$

$$= 2^{N-1}\sigma^2 \left(I_{LSB}\right) + \left(2^{N-1} - 1\right)\sigma^2 \left(I_{LSB}\right) = \tag{5.4}$$

$$= \left(2^N - 1\right)\sigma^2 \left(I_{LSB}\right) \tag{5.5}$$

Therefore, considering that two mirrors are switching at the same time, we obtain for the standard deviation of this transition the following relationship:

$$\sigma\left(\Delta I\right) = \sqrt{2}\sqrt{2^N - 1}\frac{\sigma_{ILSB}}{I_{LSB}} LSB \tag{5.6}$$

This sigma, ΔI, is a good estimation of the DNL, which can be used to size the LSB transistor in order to let the standard deviation of the LSB current to satisfy the 0.5 LSB of DNL specification. To obtain this result two different strategy can be adopted. The most straightforward one is the increase of the device area in order to minimize the mismatch affecting the current sources. An alternative way is to implement more sophisticated switching schemes, where

the MSB are not binary weighted, but rather implemented in a thermometric way [5.1]. This second strategy allows the designer to save a large amount of silicon area, at the expense of the introduction of some digital cells to implement the conversion from binary to thermometric code. However, in this design we had no particular area specification, so a straightforward increase of the silicon area of the current sources has been chosen.
The sizing of the elementary current source M_{0b} has been obtained by means of calculations based on the mismatch data reported in the process manual and on Monte-Carlo simulations. With this approach, the LSB transistor has been sized with $W = 0.8$ µm and $L = 9$ µm. The other transistors have been scaled directly using multiplicity in a binary fashion, while M_3 has a multiplicity of 2000.
The DNL obtained from several Monte-Carlo runs is shown in Fig. 5.2. It can

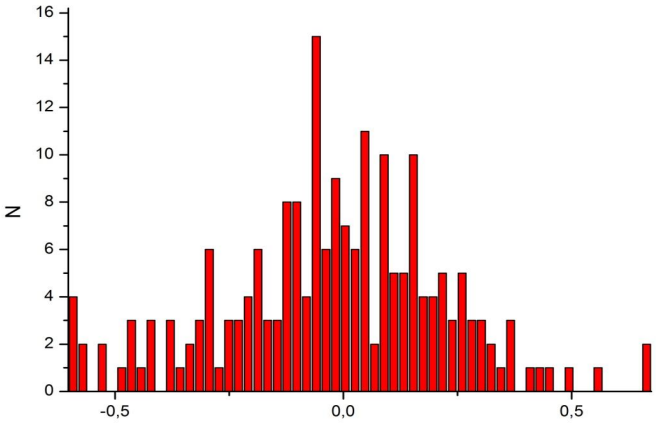

Figure 5.2: DNL estimated in correspondence of the worst-case transition.

be observed that in most cases the DNL is lower than 0.5 LSB. The standard deviations resulted to be 0.27 LSB.
Noise performances have also been investigated, obtaining an integrated noise (0-100 Hz) of 37.8 nA, when the common-mode output noise is considered, and of 5.1 nA and 9.2 nA, when the output currents are balanced or fully non-balanced, respectively. Stability of the regulator loop has also been tested. Capacitance C_{g1} represents the gate capacitance of M_1, added to that of M_3. Since M_3 and its replica are always connected and have a very large area, their gate capacitances help to stabilize the loop, which results to have a phase

margin of 80°, with no need of adding compensation capacitances.
In addition, the voltage V_{ref} can be properly chosen by means of a resistor-string DAC, in order to configure the LSB current. The robustness of the heater driver and its functionality has been tested versus temperature, different values of V_{ref} and different input codes. No particular issues have been highlighted by these simulations.

5.2 Additional blocks

The chip integrates additional blocks, necessary to the functionality of the amplifier. Particularly, chopping frequency is obtained by means of a traditional relaxation oscillator. The currents necessary to the amplifier are all obtained by a reference current generated by a δV_{gs} current reference [5.2]. The reference is compensated against corner and temperature. Process variations have been compensated adding the possibility of digital configuration of the output current, while temperature has been compensated using different material reference resistors with different values in order to nullify the temperature coefficient of the output current.
Several analog multiplexers have been also inserted, implementing several selecting functions, e.g. the sensor to be connected to the amplifier. The input terminals of the amplifier can also be routed to chip pads in order to test the interface. An *ad hoc* serial interface has been also integrated in order to let the user to configure the different functions.

5.3 Floorplan and layout of the System-on-Chip

After design and simulation phase, the layout of the blocks constituting the chip has been carried out. The layout of the entire chip is shown in Fig. 5.3. The instrumentation amplifier and the driver have been highlighted, as well as the integrated flow sensors. The three sensors are characterized by different sizing and construction. On the same chip have been integrated also other test structures, not related to this project. The large silicon space left around the sensors is necessary for proper post-processing and packaging.
The instrumentation amplifier layout is shown in Fig. 5.4. The main silicon area contributions are represented by the integrating capacitances and the preamplifier. The total area of the instrumentation amplifier is 1500x400 μm^2(0.6 mm^2), which is a very compact area for this kind of amplifiers, especially when very small bands are required.

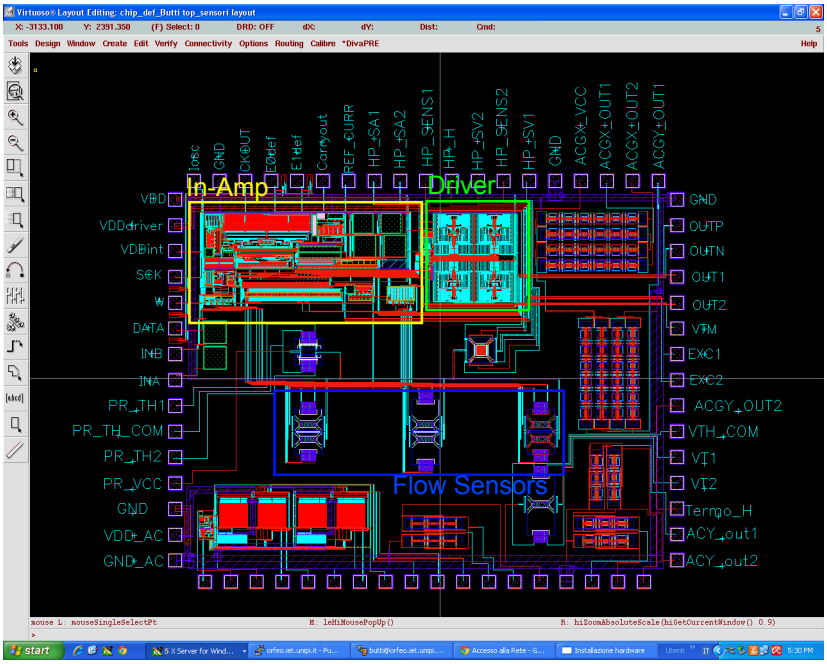

Figure 5.3: Floorplan of the System-on-Chip.

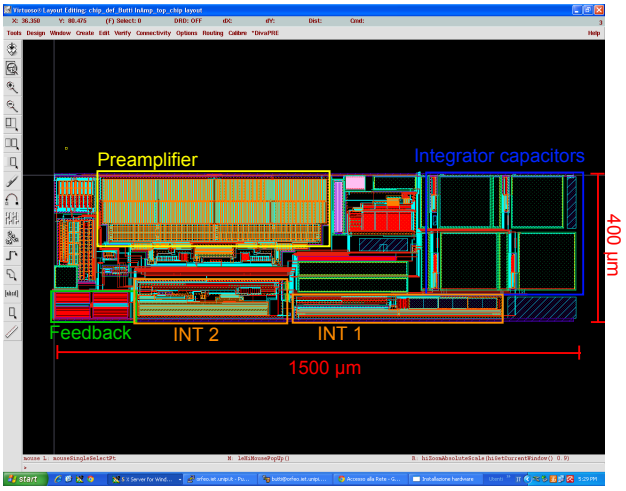

Figure 5.4: Layout of the instrumentation amplifier.

It is also interesting to look at the driver layout. Fig. 5.5 shows the layout view of a channel of the heater driver. The least significant bits have been laid

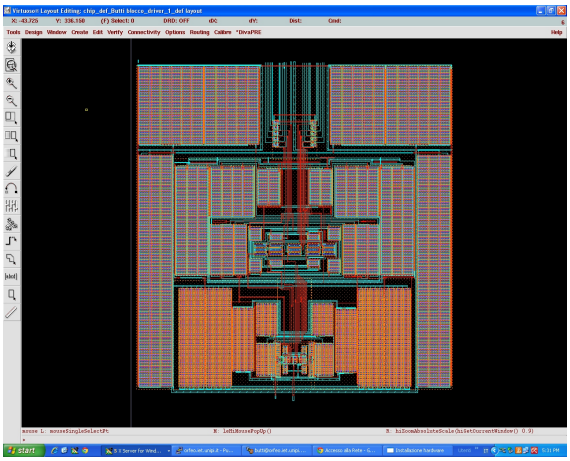

Figure 5.5: Layout of the heater driver.

out in the center of the driver. The LSB, constituted by a single device, is put in the middle of the layout. The latter is then developed building the higher order bits symmetrically around the LSB. The most significant bits are laid out trying to maintain as much as possible the symmetry of the structure, in order to mitigate the impact of the gradients, which can potentially increase the mismatch and thus the DNL of the driver.

5.4 Conclusions

The proposed instrumentation amplifier has been laid out and integrated into a complete System-on-Chip, comprising also a programmable heater driver, in order to allow the user to correct the sensor offset. The chip integrates three different flow-meters, as well as several functional blocks necessary to the proper functionality of the whole system. The layout has been completely carried out and sent to the foundry for actual fabrication.

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Chapter 6

Optimization of very low frequency G_mC integrators

The research activity presented in this chapter has been focused on the optimization of very low frequency G_mC integrators, which constitute the basic building blocks of G_mC filters. These filters play an important role in mixed-signal integrated CMOS circuits for MEMS sensor interfacing and biomedical data acquisition and processing. In these applications, as in the case of the previously discussed instrumentation amplifier, sub-kHz singularities are often required, thus leading to an increase of the silicon area devoted to the filter, especially when tight specifications are put on the dynamic range of the filter itself. In this chapter, the topic will be introduced and discussed, and optimization and automatic sizing routines developed in the MATLAB environment will be presented. Finally, the results will be discussed and some optimum design guidelines will be provided.

6.1 Introduction

In spite of the last decade trend to assign as much as possible signal processing to the digital part of an electronic system, thanks to the ever-growing integration capability, some functions have necessarily to be performed in the analog domain. Filtering is one of those. In particular, time continuous analog filtering [6.1] is mandatory e.g. for limiting the bandwidth and reject out-of-band spuries and disturbances of a signal, prior to perform the AD conversion, in order to avoid saturation of the ADC and to relax its specifications. In addi-

tion, time-continuous filter do not suffer of noise fold-over, aliasing of the signal spectrum or clock feedthrough.

G_mC filters [6.2] are the most frequently adopted category of continuous-time filters, thanks to their versatility, reduced area occupation and reduced power consumption, tunability and high frequency capability. For these reasons, they are nowadays very used in several applications, distributed along all the frequency range, from 0.1 Hz to hundred of MHz. On the high side, G_mC filters are widely used for the hard disk drive reading channels [6.3, 6.4, 6.5, 6.6], and for intermediate frequency and base-band signal processing in RF receivers [6.7, 6.8, 6.9, 6.10, 6.11]. On the low side of the frequency range, involved in the present research activity, G_mC filters are used in medical applications such as EEG or ECG and integrated low-bandwidth sensor interfacing [6.12, 6.13, 6.14, 6.15].

Typically, biomedical signals have an amplitude in the order of 100 µV-100 mV and a bandwidth of 1-100 Hz [6.16]. On the other hand, several kinds of integrated sensors, e.g. MEMS thermal sensors or other kinds of bridge sensors, exhibit output signal in the order of a few mV , with a bandwidth extended from DC to a few kHz. As a significant example, the amplifier presented in this thesis has been designed to have a bandwidth of 200 Hz, using two low frequency G_mC integrators. Design of such a low frequency singularities filter is not trivial [6.17], due to the large area required by the capacitors, especially in case of tight specifications in terms of linearity and noise level.

G_mC filters are based on the G_mC integrator, which consists in an OTA (Operational Transconductance Amplifer), with its transconductance g_m, and an integrating capacitance C. The designer can adopt various approaches to develop the filter architecture [6.18], depending on the transfer function he wishes to obtain, the expected dynamic range, the sensitivity to the circuit parameters and so on. Generally, the singularities of the filter result to be bound to the integrating constant or unity gain frequency of the building integrators, given by the ratio between the transconductance (g_m) and the capacitance (C). When very low frequency singularities are required, very small g_m/C ratios have to be implemented. This can be achieved either by choosing a very low g_m, which in turn is obtained using very long-channel transistors, or a large capacitor. Both of these approaches lead to a rapid increase of the silicon area required by the filter. Moreover, using very long transistors can cause layout issues. Dynamic range and linearity specifications can further complicate the design.

The afore-mentioned aspects have been addressed in several papers, where techniques for designing very low transconductance OTAs have been presented.

Current cancellation and current division and splitting techniques [6.19, 6.20, 6.21, 6.14] can be succesfully implemented to obtain transconductances in the nA/V range or even below, and optionally combined with source degeneration [6.22], in order to improve linearity. Another technique that can be used is the transconductance multiplication [6.23]. Floating-gate or bulk-driven transistor intrinsic gate-voltage attenuation has also been evaluated [6.20]. A different approach consists in biasing the input transistors in the triode region, where the lowest ratio g_m/I_d is achieved [6.24]. In this way, it is possible to design very low g_m and easy to tune transconductors, without incurring in the lower limit of the biasing current imposed by leakage consideration, as in the case of weak-inversion operation [6.25]. On the other hand, to mitigate the area impact of the required large capacitances, impedance scaling techniques have been developed and presented [6.21].

All of the mentioned techniques present their own advantages and limits in terms of achievable g_m/C ratio, dynamic range, noise performances, linearity range and THD, offset and area occupation. For this reason, a deepened investigation of trade-offs should be performed in order to satisfy all the specifications and achieve an optimal design. The large variety of degrees of freedom and the tightness of the constraint can complicate or even make ineffective an analytical approach. Therefore, numerical analysis can be exploited in order to optimize the design and deal with the complexity of the problem. Several architectural approaches aiming to the optimization of the G_mC filters can be found in the literature [6.26, 6.27, 6.28], usually relying on state-space representation of the filters and trying to meet the design contraint through the optimization of the system architecture. Actually, for the system-level approach to be effective, it has to be complemented with an optimum sizing of the basic builing blocks of the G_mC filter, i.e. the integrator. To the author's knowledge, few works in the literature deal with the optimization of the G_mC integrator [6.29], in particular when the silicon area of very low frequency integrators is taken into account as the target of the optimization itself. A numerical routine, capable of operating an automated transistor-level sizing of a G_mC integrator while satisfying several constraints and minimizing area occupatin, has been developed in the MATLAB® environment, exploiting functions of the Optimization Toolbox. The routine can be configured with the parameters of commercial technological CMOS processes and aims to support the design activity, providing a good starting point, which can be furtherly refined by the designer with the help of an electrical simulator. Morevore, several tests have been performed in order to define some general and useful guidelines for the design of optimum

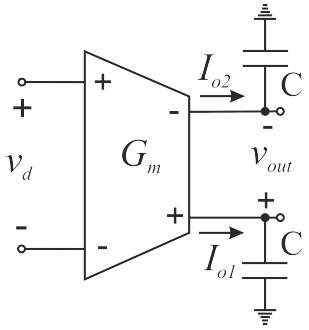

Figure 6.1: Fully differential G_mC integrator

very low frequency G_mC integrators, such as the ideal amount of silicon area to assign to the transconductor and to the capacitor and the use of very large current division factors. These guidelines have also been partially exploited in the design of the presented instrumentation amplifier.

6.2 Integrator topology and modelling

A typical fully-differential G_mC integrator is shown in Fig. 6.1. The transconductance G_m is defined as:

$$G_m = \frac{I_o}{v_d} = \frac{I_1 - I_2}{v_d} \tag{6.1}$$

and the output voltage in the Laplace domain $v_{out}(s)$ can be written:

$$v_{out}(s) = \frac{\omega_0}{s} v_d(s) \tag{6.2}$$

where s is the Laplace complex variable and the unity-gain pulsation ω_0 is given by:

$$\omega_0 = \frac{G_m}{C} \tag{6.3}$$

The unity-gain frequency f_0 can be as well defined as $2\pi\omega_0$.
Among the topologies afore-mentioned and described in the bibliography, the focus has been put on a transconductor based on the pseudo-differential pair, shown in Fig.6.2. The differential input v_d is defined as $v_1 - v_2$ and I_{o1} and I_{o2} are the output currents. Transistors M_1 and M_2 implement the pseudo-differential pair and perform the voltage-to-current conversion. Transistors M_3-M_5 and M_4-M_6 constitute the current mirror load, which transfers to the output the differential current from the pair. The mirror ratio K_m is defined as $I_{d5}/I_{d3} = I_{d6}/I_{d4}$. This coefficient is usually chosen lower than 1 in low

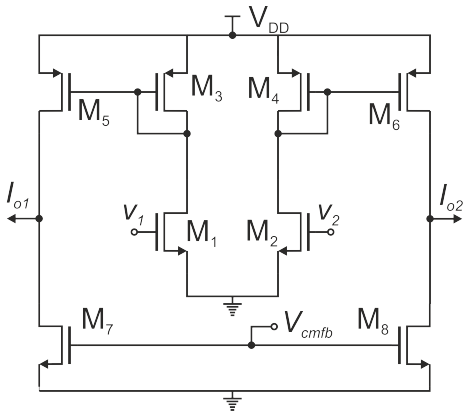

Figure 6.2: Fully differential transconductor based on a pseudo-differential pair.

frequency applications, to reduce the overall transconductance. The impact of this choice on area occupation will be evaluated later in this chapter. The terminal V_{cmfb} has to be connected to a common-mode feedback, driving the gate of M_7-M_8 in order to stabilize the output common-mode voltage to the desired value. The output differential current can then be written as:

$$I_o = I_{o1} - I_{o2} = K_m G_{m1} v_d \tag{6.4}$$

where G_{m1} is the transconductance of M_1 and M_2 and, if the transistors are biased in saturation region, is given by:

$$G_{m1} = \beta \left(V_{gs} - V_{TH} \right) \tag{6.5}$$

with $\beta = \mu_n C_{ox} W/L$. Saturation region has been chosen for the transconductor operation, as the noise performances are better with respect to triode region. The pseudo-differential pair results to be very attractive for low voltage applications, since it requires no tail current source, which would decrease the maximum input common-mode swing, due to its headroom voltage. However, this results into a very poor rejection of the input common mode. Actually, the common-mode transconductance is equal to the differential transconductance, i.e. $K_m G_{m1}$. For this reason, variations of the input common-mode can lead to large variations of the output common-mode. The CMFB circuit used to stabilize the latter should then be robust and fast. Furthermore, the large common-mode transconductance can increase the gain of common-mode positive feedback loops in some filter topologies, leading to instability. This aspect has been addressed in [6.5], where an additional feedforward transconductor is

used to cancel out the common-mode transconductance. Moreover, variations of the input common-mode directly reflect on the biasing condition of the input transistors, changing their small signal parameters and, as a consequence, the transconductance G_m. These problems can be mitigated if the input common-mode does not varies. This is a typical situation in fully-differential systems, where the output common-mode of a previous stage is stabilized to a given value.

Another advantage of the pseudo-differential pair is represented by its large input linearity range. Taking into account a MOS differential pair and the simple square-law drain current equation, its differential output current can be written as:

$$I_d = I_o \frac{v_d}{V_{MAX}} \sqrt{2 - \frac{v_d^2}{V_{MAX}^2}} \tag{6.6}$$

where I_o is the bias current and $V_{MAX} = \sqrt{2I_o/\beta} = \sqrt{2}\,(V_{gs} - V_{TH})$, where $(V_{gs} - V_{TH})$ is the overdrive voltage of the pair. If a linearity error lower than 1% is required, v_d has to be lower than $0.2V_{MAX}$. As an example, with an overdrive of 250 mV, the maximum input differential voltage allowed would be equal to about 70 mV. This limitation is not acceptable in several applications. On the other hand, the differential output current of a pseudo-differential pair with the transistors in saturation region can be written as:

$$\begin{aligned} I_d = \frac{\beta}{2}\,(V_{gs1} - V_{TH})^2 - \frac{\beta}{2}\,(V_{gs2} - V_{TH})^2 = \\ \frac{\beta}{2}\,(V_{gs1} + V_{gs2} - V_{TH})\,(V_{gs1} - V_{gs2}) \end{aligned} \tag{6.7}$$

Considering that:

$$V_{gs1} = V_c + \frac{v_d}{2} \tag{6.8}$$

$$V_{gs2} = V_c - \frac{v_d}{2} \tag{6.9}$$

where V_c is the input common-mode voltage, eq. 6.7 can be rewritten as:

$$I_d = \beta\,(V_c - V_{TH})\,v_d \tag{6.10}$$

The transconductance G_{m1} of the pair is then given by:

$$G_{m1} = \beta\,(V_c - V_{TH}) \tag{6.11}$$

It can be observed that the pseudo-differential pair operates in linear condition on all its working range. The maximum input differential voltage V_{dMAX} it can handle can be calculated considering that V_{gs} of a MOS transistor should be larger than V_{TH} to avoid entering weak inversion region and turning off. Then the following should hold:

$$V_c - \frac{V_d}{2} > V_{TH} \tag{6.12}$$

and

$$V_{dMAX} = 2\left(V_c - V_{TH}\right) \tag{6.13}$$

The noise performances are often one of the key specification of a filter. Using a simple model [6.30], the gate-referred flicker noise PSD (Power Spectral Density) of a MOS transistor $S_{vf}(f)$ can be written:

$$S_{vf}(f) = \frac{N_F}{WL}\frac{1}{f} \tag{6.14}$$

where N_F is a process-dependent coefficient. Then, the flicker noise component of the input-referred noise PSD of the transconductor of Fig. 6.2 can be obtained:

$$S_{vf}(f) = 2\frac{1}{f}\left[\frac{N_{Fn}}{W_1 L_1} + F_3^2 N_{Fp}\left(\frac{1}{W_3 L_3} + \frac{1}{W_5 L_5}\right) + \frac{F_7^2 N_{Fn}}{W_7 L_7}\right] \tag{6.15}$$

where N_{Fn} and N_{Fp} are the flicker noise coefficients of the NMOS and the PMOS, respectively. Factors F_3 and F_7 are defined as:

$$F_3 = \frac{V_{gs1} - V_{TH}}{V_{gs3} - V_{TH}} \tag{6.16}$$

$$F_7 = \frac{V_{gs1} - V_{TH}}{V_{gs7} - V_{TH}} \tag{6.17}$$

The transconductor input-referred thermal noise PSD S_{vth} can be also calculated:

$$S_{vth} = \frac{8}{3}\frac{kT}{G_m}\left[K_m + F_3\left(K_m + 1\right) + F_7\right] \tag{6.18}$$

Although constraint can be independently put on thermal and flicker noise, it is more useful from an application point of view to take into account the input *rms* noise, calculated integrating the total noise PSD over a frequency band of interest B:

$$v_{in-rms} = \sqrt{S_{vth}B + S_{vf}\left(f\right)\ln\left(\frac{f_H}{f_L}\right)} \tag{6.19}$$

where f_H and f_L are the upper and lower limit of the band B. Usually, the unity-gain frequency f_0 is taken as f_H for the G_mC integrators. The dynamic range DR of the integrator can be defined as:

$$DR = \frac{\text{max signal}}{\text{peak} - \text{to} - \text{peak noise}} = \frac{V_{dMAX}}{4v_{in-rms}} \tag{6.20}$$

where a crest factor of 2 has been assumed for the noise.

6.2.1 Optimization for minimum area occupation

One of the main concerns when dealing with very low frequency G_mC integrators is the increase of silicon area required to meet the specifications. The integrator overall area A_{tot} can be written as:

$$A_{tot} = A_{OTA} + 2A_{CAP} \tag{6.21}$$

where A_{OTA} is the area of the transconductor and can be approximated summing up the MOSFET gate areas:

$$A_{OTA} = 2\left(W_1L_1 + W_3L_3 + W_5L_5 + W_7L_7\right) \tag{6.22}$$

and A_{CAP} is the integrating capacitance area, which can be related to the transconductance G_m:

$$A_{CAP} = \frac{G_m}{k_c}\frac{1}{2\pi f_0} \tag{6.23}$$

where k_c is a process dependent parameter, representing the capacitance per unit area. As stated before, the reduction of f_0 requires either to reduce G_m and to increase C. The latter results into a proportional increase of the area occupation. The area impact of a straight-forward decrease of G_m can be also described. Let us consider a minimum size MOS transistor (namely with minimum width W_{min} and length L_{min}), biased at a given overdrive voltage in the order of a few hundred of mV, as often required, due to the input swing. In these conditions, the MOS transconductance g_m is usually a few orders of magnitude larger than those required to implement very low unity-gain frequencies in G_mC integrators. It is then necessary to choose a W/L ratio much lower than 1. The most area efficient way to do that is to choose W_{min} for the width and to increase the channel length. Eq. 6.5 can then be

rearranged to put in evidence the gate area $A_1 = W_{min}L_1$:

$$G_{m1} = \mu_n C_{ox} \frac{W_{min}}{L_1} (V_{gs1} - V_{TH}) = \mu_n C_{ox} \frac{W_{min}^2}{A_1} (V_{gs1} - V_{TH}) \tag{6.24}$$

It can be observed that if the required G_{m1} is lower than the transconductance achieved with a minimum size MOS at a given overdrive voltage, the gate area results to be inversely proportional to G_{m1}. As Eq. 6.4 suggests, a mirror ratio $K_m \ll 1$ can be selected, in order to relax the specification on G_{m1}. However, making this choice implies that the lenght of the output transistors $M_5 - M_6$ and $M_7 - M_8$ has to be proportionally increased, in order to obtain W/L ratios low enough to handle such a low current. With the simplifying assumption of all the transistors widths set to W_{min}, it can be shown that the integrator area is asimptotically minimized when K_m tends to 0. Thus, it seems to be convenient to set K_m to a very small value. As an example, in [6.19], K_m is chosen equal to $2.5 \cdot 10^{-6}$. With this assumption, A_{OTA} results actually to be inversely proportional to G_m, while A_{CAP} is proportional to the latter. Using these arguments, an optimum value for G_m, which minimizes the integrator area, can be found with simple analytical steps. An A_{tot} proportional to $f_0^{-0.5}$ comes out, as also stated in [6.19]. It should be observed that in this simplified case no constraints on noise have been taken into account. Noise specifications however strongly affects the area occupation of the cell. Flicker noise constraint requires to increase the gate area of the transistors, in such a way that the channel width cannot be set to the minimum. On the other hand, thermal noise is directly related to the G_m of the transconductor. Actually, it is always possible to write the input referred thermal noise PSD of an integrator, S_{TH}, as [6.29]:

$$S_{TH} = \frac{4kT\xi}{G_m} \tag{6.25}$$

where k is the Bolztmann's constant, T the absolute temperature and ξ is the integrator noise factor, which has a value greater than 1 and depends on the topology of the circuit. It is clear that to reduce S_{TH} it is necessary to increase G_m. This leads, in turn, to an increase of C, to meet the frequency specification, with area penalization. The strong interaction between frequency, input range and noise constraints makes unpractical an analytical approach to the optimization of the integrator, which cannot be easily and effectively performed without simplificative assumption that can lead to widely non optimal cells. The numerical approach presented here has been developed to help the designer to overcome the issues presented by the constraint interaction.

6.3 Optimization routine for integrator design

The optimization routine has been developed in the MATLAB^{TM} environment, using the function *fmincon* from the Optimization Toolbox [6.31]. The *fmincon* minimizes an objective function with respect to linear and non-linear constrains, choosing the optimum values of a given set of degress of freedom (DOFs) and it is based on the Sequential Quadratic Programming (SQP) algorithm. Upper and lower bounds of the DOFs have also to be provided to the function. Thanks to this features, the *fmincon* function is particularly suitable to be used to perform an automated sizing of analog circuts, provided that they can be completely described by a set of analytical equations.
All the circuit parameters characterizing the integrator circuit presented in 6.2 can be obtained by means of the presented equations if the following set of DOFs x_{DOF} is chosen:

$$x_{DOF} = (W_1, L_1, W_3, L_3, W_5, L_5, W_7, L_7, V_{d\max}) \tag{6.26}$$

Upper and lower bounds in this case are suggested by technology limitations (W_{min},L_{min}) or feasibility considerations (L_{max}), except for $V_{d\max}$, which is an actual design specification. Since we are interested in minimizing the area for low frequency application, Eq. 6.21 is taken as the objective function. The primary design constraint has been chosen to be the *rms* noise value, given by 6.19, due to its relevancy in defining the filter permormances, and, together with $V_{d\max}$, its dynamic range. Other constraints are also introduced on the overdrive voltages of the transistors, to comply with the supply voltage and to assure to remain in the saturation region of operation. The integrator unity-gain of intereset (f_0) has to be entered by the designer when the routine is invoked, and is used by the program as a given parameter. The program requires also a starting point x_0. At the end of the iteration, if the value of the constraints are consistent with the search domain represented by the DOFs bounds and convergency can be achieved, the routine returns the minimum total area A_{tot}, the transconductor area A_{ota}, the capacitor area A_{cap}, with the selected optimum value for all the degrees of freedom.
As the SQP minimization algorithm is an analytical optimization method, it is subjected to the possibility of being stuck in local minima. This aspect has been taken into account: several optimization runs are started from randomly generated starting point belonging to the search domain, and the best result is taken as the minimum.

The presented routine can be configured to work with different CMOS technologies: the designer has to provide the value of a limited set of process dependent parameters, as the minimum length and width L_{min} and W_{min}, hole and electron mobilities μ_p and μ_n, C_{ox}, k_{cap}.

6.3.1 Optimization results

The routine has been configured with the process parameters of the 0.32 µm - 3.3 V BCD6s STMicrolectronics process. In all the presented tests, $V_{d\mathrm{MAX}}$ minimum value has been chosen to be 1 V. The upper frequency limit f_H of the band of interest B is chosen as f_0, whereas the lower limit f_L is given by 0.01 Hz.

As a first test, optimization routine has been run disabling the noise constraint, so that only f_0, together with the DOFs bounds, plays a role in determining the minimum required amount of silicon area. The resulting trend of A_{tot}, A_{cap} and A_{ota} when f_0 is swept from 5 Hz to 10 kHz and no noise constraints are enabled are represented in Fig. 6.3(a). It can be noted that the routine sets A_{cap}

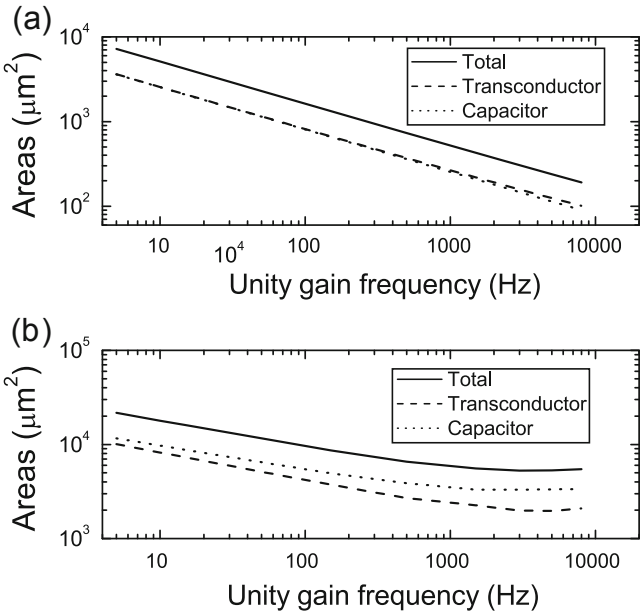

Figure 6.3: Optimized areas as a function of f_0 when no noise constraint are enabled (a) and when a maximum v_{in-rms} of 30 µV is required (b), after [6.32]

and A_{ota} to an equal value. Moreover, a dependency of A_{tot} on around $f_0^{-0.5}$ can be observed. This confirms the arguments given in the previous section and in previous studies [6.19]. Unfortunately, this situation is not fully representative of an actual design, since no noise constraints are taken into account.

Fig. 6.3(b) shows the results of the same experiment, run when a maximum v_{in-rms} of 30 µVis acceptable. The noise constraint clearly alters the area trends: the dependency on the frequency remains valid only below approximately 1 kHz, whereas for higher frequencies the noise constraint dominates and the trend canges. Another clearly visible effect is the difference between transconductor and capacitor areas. The latter is larger over all the frequency range, particularly on the high side, but still it is 20% larger also at the lowest investigated frequency (5 Hz). Finally, the obtained A_{tot} values are decisively larger than those reported in Fig. 6.3(a). Thus, neglecting the noise impact, even at low frequencies, can be completely misleading in looking for optimum design criteria.

To gain a more deepened view of the noise effect, optimization tests have been run progressively decreasing the noise level from 10 mV to 4.5 µV, with f_0 set to 100 Hz. Fig. 6.4 shows the results. The most relevant aspect to point out

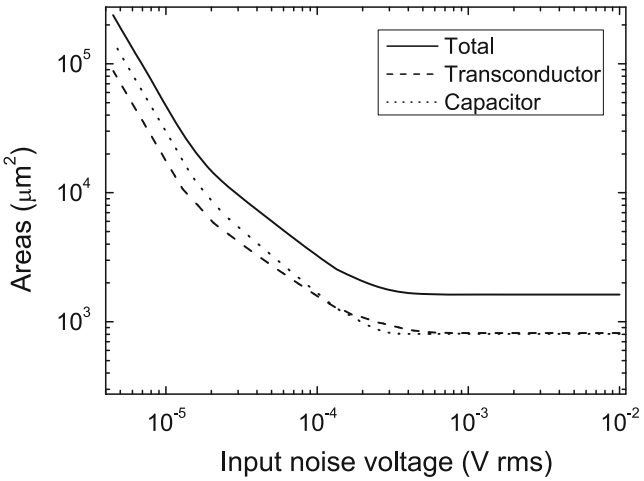

Figure 6.4: Optimized areas as a function of v_{in-rms} with $f_0 = 100$Hz, after [6.32].

is the significant area increase taking place when the noise constraint tightens. This is in complete agreement with the arguements discussed in section 6.2: the routine decisively increases the overall transconductance G_m, to reduce the thermal noise PSD (see Eq. 6.25). This, in turn, requires a proportional increase of C in order to meet f_0 specification. The transconductor area A_{ota} is also increased, even if at a lower pace, in order to counteract flicker noise. In fact, the percentage of area occupied by the capacitor passes from 50% when the noise constraint is relaxed, as previously shown in Fig. 6.3 to 63% when

the noise constraint becomes stricter.
It is important to note that Figs. 6.3 and 6.4 have been obtained with no upper bounds on the transistor lengths. This leads to very long channel transistors ($L \geq 2.5mm$), which can result to be unfeasible and unpractical, due to layout issues or channel leakage, or even unreliable, due to lack of characterization of such long channel transistors in the process design kit. This problem can be partially mitigated implementing the current mirror using series-parallel connected transistors, as described in [6.33]. The solution described in this paper is effective also from the offset point of view, which hasn't been taken into account in this work.
If an upper bound on the channel length is set, a significant area penalization comes out. Several optimization runs with progressively stricter upper bounds on the length have shown that an overall increase of the integrator area is required to meet the specifications. In particular, A_{cap} becomes even more important than in the previous cases, reaching a percentage of 85% of the total area if L_{max} is set to 500 µm [6.32], because the routine has to increase the width of the transistors to compensate for the increase of flicker noise. In turn, G_m increases, and C has to be increased as well.
Another interesting aspect that can be evaluated is the role played by the different components of the noise PSD, thermal and flicker. Actually, flicker noise can be effectively removed if techniques such as chopper modulation are applied, as in the instrumentation amplifier described in the previous chapters. To evaluate the advantage in terms of area that can be obtained, the optimization tests described before have been repeated disabling the flicker noise. Fig. 6.5 summarizes the results, showing A_{tot}, A_{cap} and A_{ota} when f_0 is swept from 5 Hz to 10 kHz and a noise constraint of 30 µV is set, as in the case of Fig. 6.3. The figure also shows the total area in case of both thermal and flicker noise are enabled for comparison. It is clear that removing flicker noise helps to save silicon area, up to 40% when f_0 is lower than 1 kHz. Furthermore, A_{cap} dominance is even more marked, since in this case the transconductor area plays no direct roles in determining the noise performances, which are determined mainly by G_m. As in the previous case, the trend of the areas when the noise constraint is swept and f_0 is fixed to 100 Hz has been investigated. Fig. 6.6 shows the results. It can be observed that A_{ota} is not monotonically dependent on the noise constraint. This is due to the way the routine tries to meet the specification. Initially, when the noise constraint is not effective, areas remain flat. Then, as the constraint tightens, A_{ota} decreases, due to the reduction of the length of M1 necessary to increase G_m. The subsequent increase is caused

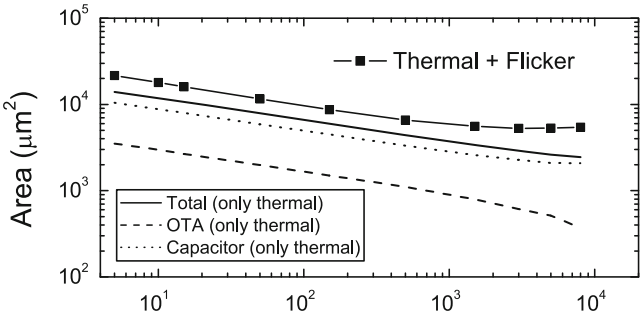

Figure 6.5: Optimized areas as a function of f_0 with 30 μV *rms* noise constraint and only thermal noise is considered. Total area in case of both flicker and thermal noise PSD enabled is also shown (*squares*) for comparison, after [6.32].

by the increase of $L_{3,5,7}$, operated to increase the overdrive voltage of $M_{3,5,7}$, respectively. This guarantees a noise reduction decreasing the noise factor ξ (see Eq. 6.25) without increasing G_m, as shown by Eqns. 6.15 and 6.18. When the overdrive voltages upper limit, in this case set to 0.75 V, is reached, A_{ota} is again decreased through the reduction of all devices length, operated to increase decisively G_m. Although this may seem weird, the routine suggests it as the optimum way to meet the constraint at a very low noise level, where we can note a reduction of the overall area of around 50% with respect to the previous case, when flicker noise was active. The last aspect taken into account

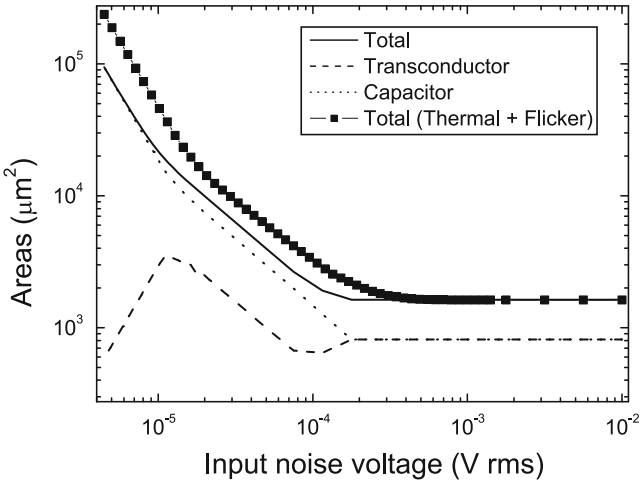

Figure 6.6: Optimized areas trend versus thermal noise constraint when f_0 is set to 100 Hz. Total area in the case of active flicker constraint is also shown for comparison, after [6.32].

is the role of the current mirror ratio K_m. As suggested by the preliminary analysis and by several previous works aforementioned, its value should always

be put to the minimum value allowed (10^{-4}) in the routine. Actually, in all the previous tests K_m was consistently close to its minimum, but at the same time large random oscillations of its value, spanning over one order of magnitude, has been observed. It is important also to note that these oscillations do not reflect onto the area curves. This behaviour suggested to further investigate this aspect. To do that, optimization runs have been performed setting K_m to a fixed value, which has then been swept from 10^{-3} to 1, while f_0 has been set to 100 Hz. Fig. 6.7 shows the result obtained when a noise constraint of 3

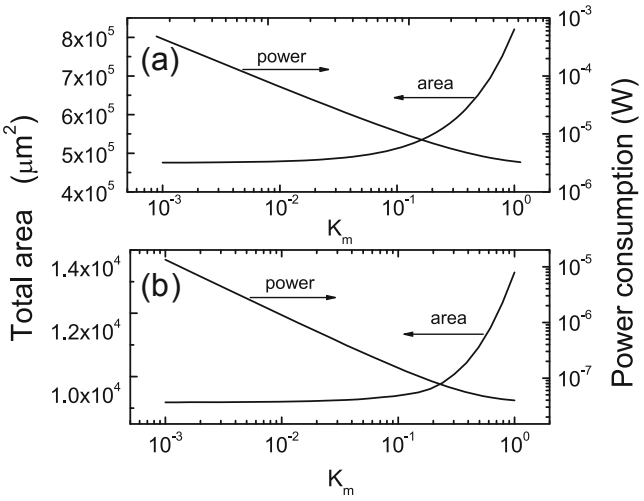

Figure 6.7: Optimized total area and power dissipation versus K_m over a 0.01-100 Hz bandwidth. Noise constraint is set to 3 μV*rms* (a) and to 30 μV*rms* (b), after [6.32].

μV *rms* (a) or 30 μV*rms* (b) is set. It can be quite surprisingly observed that an area reduction of only 40% is achieved over three decades of K_m reduction. Furthermore, the area value does not change significantly below 10^{-1}, while, on the other hand, the power consumption increases. This can be ascribed to side effects related to the way the optimization procedure acts to satisfy the given bounds and constraints. In fact, a too low current into the output branch would result in too long transistors, with penalization in terms of area and feasibiity. Thus, the decrease of the output current is opposed by the routine, which at a certain point starts to increase the current into the input section to satisfy the constraint onto K_m.

6.3.2 Routine accuracy

The routine has been primarily used to define some design criteria for low frequency G_mC integrators, when different constraints are taken into account,

especially noise performances. However, the accuracy of the routine has been tested to verify whether it could be used for actual sizing of a circuit or the obtained paramaters needed some refinement to exactly match the specifications. To this purpose, several optimization runs have been performed and the obtained sizing has been tested by means of accurate electrical simulation, performed with ELDO® (Mentor Graphics) and using device models from the commercial STMicroelectronics process BCD6s. The lower bounds of MOS width and length has been set to 0.5 µm and 0.35 µm, respectively.
Integrators with four different f_0 between 10 and 500 Hz have been automatically sized. The input noise has been put to three different values, namely 20, 30 and 75 µV *rms*, for 12 different design cases. The minimum $V_{d\max}$ has been set to 1 V, and the maximum overdrive voltage to 0.75 V. Finally, K_m value has been set to 0.05, as suggested by Fig. 6.7. The parameters returned from the routine have been directly transferred into the Cadence Virtuoso® schematic editor, and simulations have been run to estimate f_0 and the *rms* noise level. The relative differences between nominal and simulated f_0 and *rms* noise voltage are shown in Fig. 6.8. The simplified equations used in the routine lead to an underestimation of the noise level, while they overestimate f_0. The maximum difference of the former can be quantified in 75 % while that of the latter in -45%. Actually, the procedure tends to generally underestimate the MOSFET G_m with respect to the simulated values. It is clear that the values

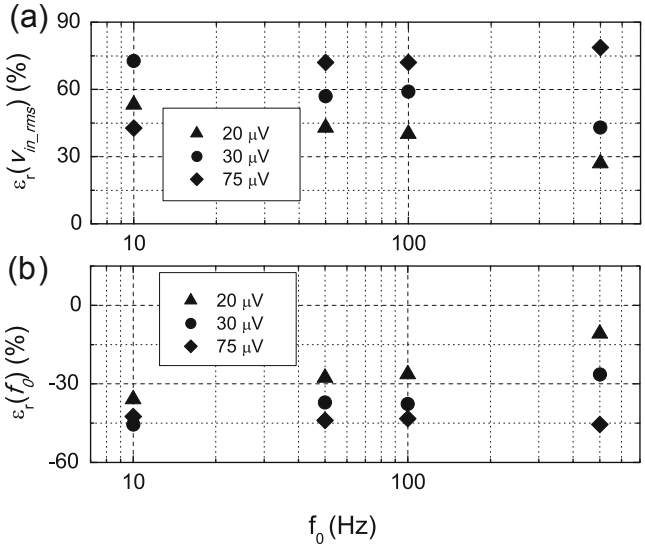

Figure 6.8: Relative difference between simulated and specifications of the integrators synthesized by the proposed procedure. Noise performance (a) and unity gain frequency f_0 (b) are reported, after [6.32].

returned by the routine are not directly suitable to design an accurate block. To overcome this issue, a two-step semi-automatic refinement procedure has been proposed in [6.32]. This approach has led to a significant improvement of the noise prediction accuracy, down to an error of only ±13%. However, f_0 has still to be fixed by the designer, choosing the appropriate capacitance value to meet the G_m/C ratio, making this approach still not completely practical.

6.4 Routine refinement and accuracy improvement

In this section a version of the routine, improved in terms of accuracy, will be presented. To this purpose, a more precise MOSFET drain current equation has been used, including effective channel width and length and mobility degradation due to the vertical field.
The previous sections have shown that the optmization routine tends, in absence of significant constraints on flicker noise, to put the transistor width W to the minimum allowed value. In submicron processes a correction factor has to be taken into account to avoid losing accuracy. Thus, the effective width W_{eff} can be written as:

$$W_{eff} = W - 2W_n \tag{6.27}$$

where W is the MOS drawn width and W_n is the reduction of the channel width due to the diffusion of the channel-stop dopant ions. In a similar manner, also the length has to be corrected:

$$L_{eff} = L - 2L_{ov} \tag{6.28}$$

where L is the MOS drawn length and L_{ov} is the gate-source/drain overlap. It can be observed that the correction of W is more significant, because in low frequency G_mC integrators narrow but long transistors are usually necessary. Both W_n and L_{ov} are process dependent and have to be passed at the routine as configuration parameters.
Another important phenomenon to be taken into account is the mobility degradation due to the vertical field. The drain current I_d can then be rewritten:

$$I_d = \frac{\beta}{1 + \theta_1 (V_{GS} - V_{TH})} \frac{(V_{GS} - V_{TH})^2}{2\alpha} \tag{6.29}$$

where θ_1 is a process-dependent parameter and α is a parameter greater than 1 [6.34]. Choosing a value of one for α is equivalent to assume a constant depletion region depth along the channel, leading to the parabolic I_d equation. This generally leads to overestimation of the drain current, thus a value smaller than 1 should be chosen. The transconductance g_m of the MOS transistors can then be evaluated:

$$g_m = \frac{2I_d}{V_{GS} - V_{TH}} \left[1 - \frac{1}{2} \frac{\theta_1 \left(V_{GS} - V_{TH} \right)}{1 + \theta_1 \left(V_{GS} - V_{TH} \right)} \right] \tag{6.30}$$

In these equations, channel length modulation and velocity saturation have not been taken into account. Actually, these phenomena are negligible for very long transistors, as those that are used in this kind of applications.
The thermal noise PSD contribution can also be refined introducing a process dependent parameter Γ and considering the body transconductance g_{mb} contribution:

$$S_{vth} = \frac{8}{3} \frac{kT}{g_m} \Gamma \left(1 + \eta \right) \tag{6.31}$$

where η is given by g_{mb}/g_m. Using these improved equations, the circuit analyis described above has been refined and the routine code has been modified. Another major change operated regards the main constraint applied: in the previous version of the routine the *rms* noise value was taken into account, while in this version the dynamic range DR, defined in Eq. 6.20 is taken into account. In this way, the input linearity range $V_{d\max}$ becomes an actual DOF. Due to the introduction of the described parameters, some configuration steps have been necessary before running the routine. It has been configured using the parameters of the BCD6s 0.32 µm 3.3 V STMicroelectronics process. Philips MOS9 models, using more complicated equations for I_d and thermal noise, were provided. For this reason, some preliminary tests have been performed in order to find the values of α, Γ and η allowing to fit the electrical simulation data. These tests have been repeated for several devices of different size, biased in saturation region, and have shown that using α equal to 1.2 a satisfactory match between the drain current value calculated from Eq. 6.29 and the simulated data could be obtained in most cases. On the other hand, η and Γ parameters have been chosen equal to 0.33 and 1.4, respectively, to fit the thermal noise level. Flicker noise parameters N_{Fn} and N_{Fp} and mobility degradation parameter θ_1 have been found into the model files. This configuration step can be repeated for other technological processes with different device models.

To perform the optimization runs, constraints have also been imposed on the MOSFET overdrive voltages, forced in the range 0.2-1 V, in order to guarantee strong inversion operation and, at the same time, compliance with the chosen 3.3 V power supply. As far as the geometrical constraints are concerned, lower bounds of 0.7 µm and 1.5 µm to W and L, respectively, in order to reduce the effect of channel dimensions on the threshold voltage V_{TH}. The accuracy of the routine has been improved by this choice. Length and width upper bounds of 1 mm have been introduced for feasibility reasons.
The results of the optimization runs confirmed what observed exploiting the previous version of the routine. The program tends to put the input linearity range to the maximum allowed value in almost all cases and then tries to minimize the noise until the DR specification is met. Fig. 6.9 shows A_{cap}, A_{OTA} and A_{tot} when the DR is swept from 250 (48 dB) to $65 \cdot 10^3$ (96 dB) for a given f_0 equal to 1 kHz (a) and to 10 Hz (b). It is interesting to no-

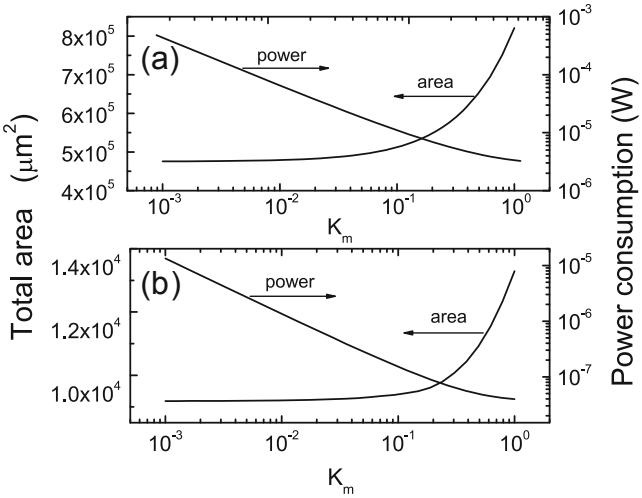

Figure 6.9: Area trends when DR is swept between 250 and $65 \cdot 10^3$ in case of f_0 equal to 1 kHz (a) and to 10 Hz (b), after [6.35].

tice that as in the case of Fig. 6.4 two different regions can be identified: for low DRs, the total area remains constant, whereas for higher DRs it begins to significantly increase. This means that when the dynamic range constraint is not really effective, the area occupation is determined mainly by the required f_0 and depends on the feasibility bounds imposed on length and width of the transistors. Then, when the DR starts to play a role, the area decisively increase, rapidly reaching large values, especially in the case of f_0 equal to 10 Hz. This behaviour has been extensively discussed in previous sections. If the area partition is taken into account, it can be observed that in case of f_0 equal

to 1 kHz A_{cap} and A_{OTA} are initially equal, then the capacitor area starts to slightly dominates. This happens because at low DRs for this f_0 DOF bounds are not hit, and the routine can freely size the circuit. The situation is different in case of f_0 equal to 10 Hz, when the capacitance largely dominates over all the DR range. This because the imposition of very low unity gain frequency requires C to be increased.

The behaviour discussed here can be clarified putting in evidence how the noise contribution are treated by the routine, as in Fig. 6.10, where the integrated contributes to the *rms* input noise are shown. In case of f_0 equal to 1 kHz the

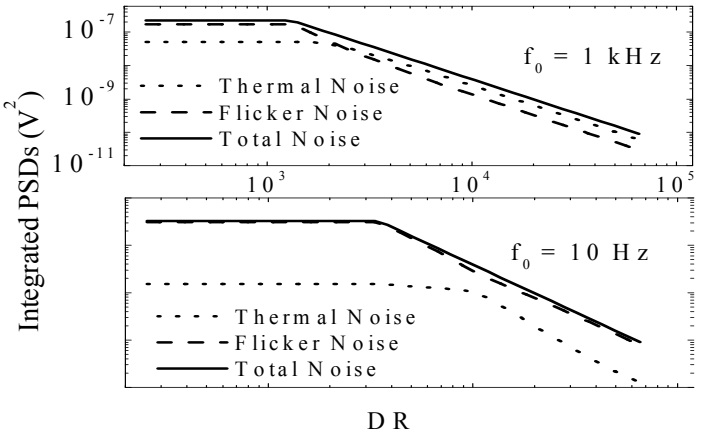

Figure 6.10: Integrated PSD contributions, thermal and flicker, to the *rms* input noise voltage obtained by the routine when DR is swept from 250 to $65 \cdot 10^3$ in case of f_0 equal to 1 kHz (a) and to 10 Hz (b), after [6.35].

thermal contribution is dominant when an high DR is required. Actually, it should be reminded that the noise bandwidth of the integrator is usually intended as extended to f_0. This explains why the thermal noise is dominant in this case. Being the f_0 specification not so tight, it is possible to increase G_m to reduce noise. On the other hand, in case of f_0 equal to 10 Hz, the flicker noise dominates over all the DR range.

Several optimization runs have then been performed to verify that the K_m trend would not change, also in the case of improved equations. The observed behaviour was very similar to that discussed above.

Finally, the procedure accuracy has been tested in a similar manner than for the previous routine version, simulating with ELDO the sizing returned by the routine. Several optimization runs have been performed, with f_0 equal to 10, 100 and 1000 Hz, and DR ranging from 200 to $7.5\Delta10^4$. The results are shown in Fig. 6.11. The relative error on the unity gain frequency $\epsilon_r\,(f_0)$ is lower than 10% in most cases and is mainly due to the K_m errors. Actually,

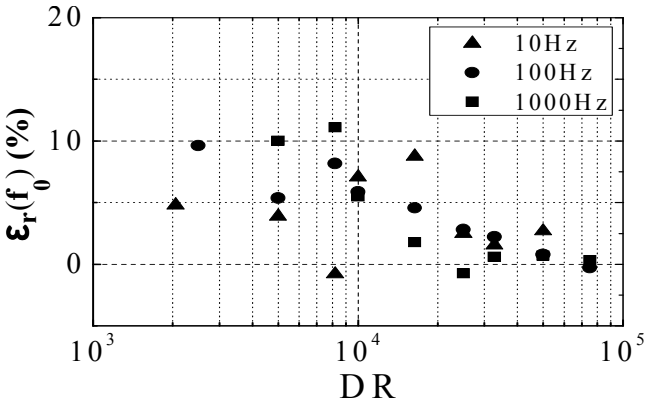

Figure 6.11: Relative error $\epsilon_r(f_0)$ on the unity gain frequency of the simulated integrator

no constraint on the current mirror have been set. Thus, the routine was free to choose different lengths for M_3 and M_5, introducing differences in channel modulation effect and in V_{TH}. The former is less relevant, due to the very long channels. The small error can be easily fixed by the designer slightly trimming the capacitance value. As far as the DR is concerned, values consistently but slightly larger (5 to 10 %) are returned by the simulations with respect to those set when the routine was run. The good accuracy achieved makes the routine an effective design tool, at least for a good starting point.

6.5 Conclusion

The proposed design procedures turned out to be effective, fast and simple tools to analyze the strong interaction between constraints on noise, linearity and area in very low frequency G_mC integrators. Some key points can be extrapoled from the described tests, valid in both cases of *rms* noise or dynamic range acting as primary constraints:

- A strong interaction intercurrs between low unity gain frequency and noise specifications that contributes to dramatically increase the occupied area. As a consequence, these two contraints cannot be treated separately in simplified analysis.

- Minimum area values are obtained if very long channel transistors (hundreds of µm or above) can be integrated. Series connection of transistors can mitigate this requirement.

- When relaxed noise specifications are given, an equal area should be as-

signed to the transconductor and the capacitors, as suggested by previous works. When the noise specifications becomes stricter, the portion of area to be assigned to the capacitors has to be rapidly increased, especially in case of bounds on transistor lengths or when only thermal noise is considered.

- Current division strategies using very small mirror coefficients (down to 10^4), sometimes proposed to reduce the area of low frequency integrators, seems to be effective only up to moderate division factors (less than 20:1), at least for what concerns the noise/frequency combinations explored. Stronger division factors seems not to produce significant effects on the cell area.

Optimally designed integrator cells for very low frequency G_mC filters can be obtained if these design hints are followed. The accuracy of the first version of the routine was not high enough to make it an actual automated sizing tool. The second version proposed, using more accurate device equations, achieves an accuracy on the given specifications better than 10% and can then be used also as a design tool, at least to define useful starting points.

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Chapter 7

Design of a compact instrumentation amplifier with high channel-gain matching for AMR sensors

The research activity described in this chapter has been carried out at NXP Semiconductors, Eindhoven, during an internship, which took place from April to December 2012. It consisted in the design of a 2-channels preamplifier for AMR bridge sensors read-out in ABCD9 technology, but fully CMOS compatible. This preamplifier is application-independent and should therefore satisfy a set of specifications obtained from several applications. It will be embedded in a complete front-end for AMR sensors for automotive applications prior to a sigma-delta switched-capacitor ADC. Therefore, high accuracy and robustness, as well as small silicon area, were required. A test-chip including the amplifier as well as a single-channel amplifier and a serial interface has been designed for testing and measurements.

7.1 Motivations

7.1.1 AMR Sensors

Anysotropic MagnetoResistance (AMR) sensors are thin-fim ferromagnetic resistive sensors whose resistance varies with the angle between the internal magnetization vector ($\vec{M}$) and the direction of the current (I) flowing through it, as shown in Fig. 7.1. The resistivity ρ of the resistor R is given by:

$$\rho = \rho_0 + \Delta\rho \cos^2 \alpha \tag{7.1}$$

The quotient $\Delta\rho/\rho_0$ is the magnetoresistive effect, usually positive, in the order of a few percent. It should be also pointed out that $\vec{M}$ in ferromagnetics materials always has its saturation value $\vec{M}_s$. When no external magnetic field $\vec{H}$ is applied, $\vec{M}$ lies along the "easy axis", i.e. the direction of lowest energy, supposed to be equal to the current direction in the figure. The latter depends on several physical parameters. When $\vec{H}$ is applied, the direction of the magnetization changes. It can be shown [7.1] that if $|\vec{H}| >> H_0$, where H_0 is called the characteristic field and depends on several physical parameters of the AMR resistor, $\vec{M}$ results to be parallel to $\vec{H}$. Otherwise, if $|\vec{H}| < H_0$, the angle γ (see Fig. 7.1) will be different than 0, i.e. $\vec{M}$ rotates less than $\vec{H}$.
The square characteristic of the AMR sensor is usually not acceptable. Linearization can be achieved with the application of slanted conductor stripes on the resistor, as shown in Fig. 7.2. The so-called barber pole structure modifies the sensor characteristics into [7.1]:

$$R(H) = R_0 \pm \Delta R \cdot \left(\frac{H_y}{H_0}\right) \cdot \sqrt{1 - \left(\frac{H_y}{H_0}\right)^2} \tag{7.2}$$

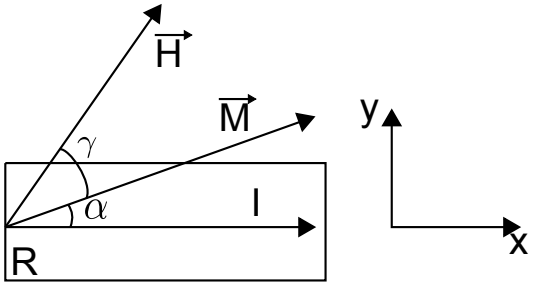

Figure 7.1: AMR resistor with $\vec{M}$, $\vec{H}$ and I directions.

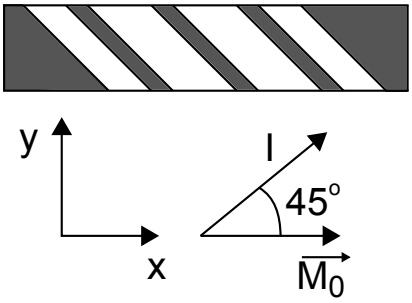

Figure 7.2: Linearized sensor employing barber poles

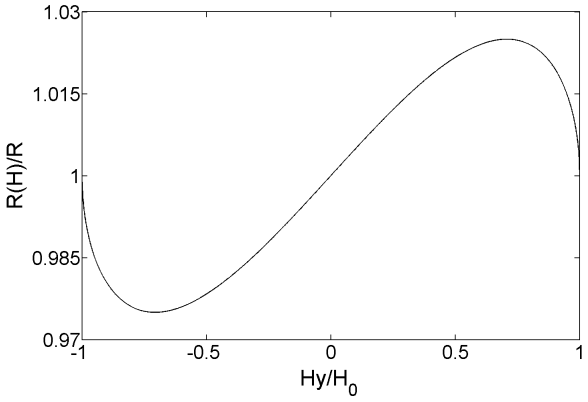

Figure 7.3: Calculated characteristic of a simple barber pole magnetoresistive sensor with $\Delta R/R$ equal to 5 %.

The characteristic is plotted in Fig. 7.3, and shows good linearity for $|H_y|<0.5H_0$, with an error lower than 5%. The sign of the slope is selected depending on the $\vec{M}$ direction. A change in its direction will produce the adoption of the other sign. This undesired behavior, referred to as "flipping" can be avoided using external H_x stabilization fields.

A complete AMR full-bridge sensor can then be built using positively and negatively inclined barber pole elements. Generally, the sensitivity S_0 of the sensor is in the y direction (or hard axis, perpendicular to the easy axis) and is defined as:

$$S_0 = \left(\frac{\Delta V_s}{\Delta H_y}\right)\frac{1}{V_0} \tag{7.3}$$

where V_s is the output voltage and V_0 is the operating voltage. The sensitivity S_0 is measured in (mV/V)/(kA/m). Using Eq. 7.2 it is possible to write the full-bridge output signal:

$$V_s \approx V_0 \cdot \frac{\Delta\rho}{\rho} \cdot \frac{H_y}{H_0}\sqrt{1-\left(\frac{H_y}{H_0}\right)^2} \tag{7.4}$$

The measuring range is defined as that field range within which the linearity error is lower than a certain quantity fixed by the application.

7.1.2 Rotational speed and angular position magnetic sensors

AMR sensors have an higher sensitivity with respect to Hall sensors. Moreover, if the external field to be sensed is higher than the saturation value or the sensor is properly biased with an additional magnet, they are sensitive only to the direction of the field to measure. Usually the measurement is accomplished using an external moving permanent magnet or by evaluating the field lines distortion caused by an iron moving part. Both principles of working are represented in Fig. 7.4. In Fig. 7.4(a) a rotating iron toothed wheel deflects the field lines

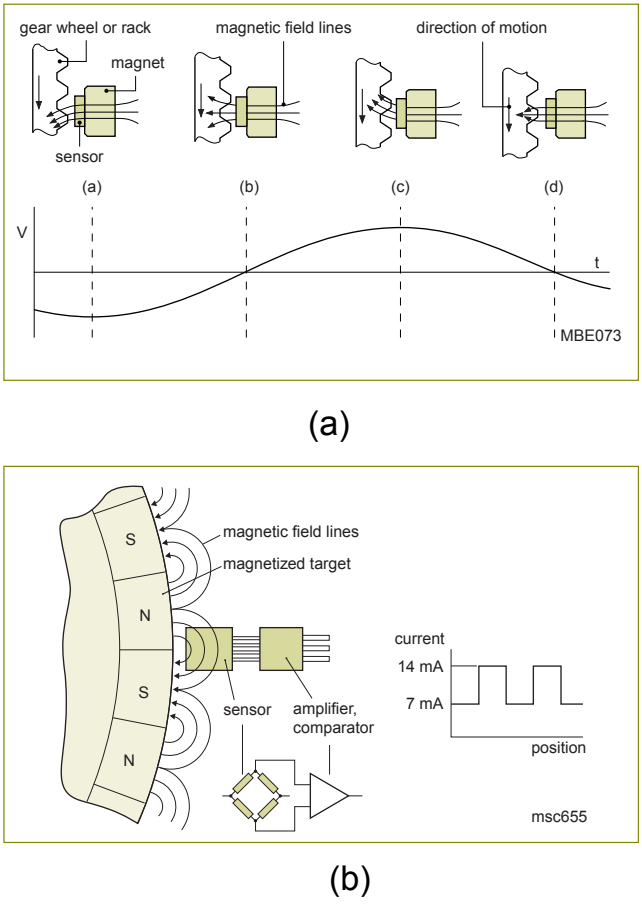

Figure 7.4: AMR sensor with passive iron moving part and biasing magnet (a) and with moving magnet (b).

produced by the back biasing magnet. The output of the bridge sensor results then to be an almost sinusoidal voltage. Counting the zero-crossing events of the bridge output voltage, it is possible to easily calculate the angular speed of the wheel. On the other hand, in Fig. 7.4(b), a magnetic rotating wheel is present, directly applying the magnetic field to the sensor. An external magnet must still be present, in order to avoid flipping. In this example, the output signal is processed by a comparator and the overall system output is a digital current, changing its value from 7 to 14 mA, depending on the magnet position. If the sensor is made by two 45° rotated full bridges, the output sinusoid waveforms will be phase shifted of 90°, due to the $\cos^2\alpha$ term in Eq. 7.1. By Analog-to-Digital conversion and subsequent digital processing is possible to perform the angle measurement. Defining V_{s1} and V_{s2} as the voltages coming out from the bridges, we have:

$$V_{s1} \propto \cos(2\alpha) \tag{7.5}$$

$$V_{s2} \propto \sin(2\alpha) \tag{7.6}$$

where α is in this case the angle between sensor and field direction and:

$$\alpha = \frac{1}{2}\arctan\left(\frac{V_{s2}}{V_{s1}}\right) \tag{7.7}$$

Due to the ambiguity inherent to the magnetoresistive effect, the expressions in Eqns. 5 and 6 are periodic with respect to α with a period of 180°, thus the angle α can only be measured from 0° to 180°. The layout of an angular sensor, namely the NXP KMZ43T, is shown in Fig. 7.5. In these sensors, it is necessary to apply an external minimum magnetic field exceeding the saturation field strength in order to guarantee reliable results. Thanks to this principle of operation, they are intrinsically robust to positioning uncertanties, vibrations and other mechanical sources of errors and can tolerate field strength variations due to ageing or temperature. AMR sensors can be succesfully employed in the automotive field, where accuracy, reliability and robustness are mandatory. Example of applications are angular sensing for electronic control of critical systems such as ABS, transmission, crankshaft or speed measurement of the steering wheel and brushless DC motors. If used in weak field conditions, AMR sensors are able to directly measure the magnetic field and find applications in compass, navigation, motion detection.

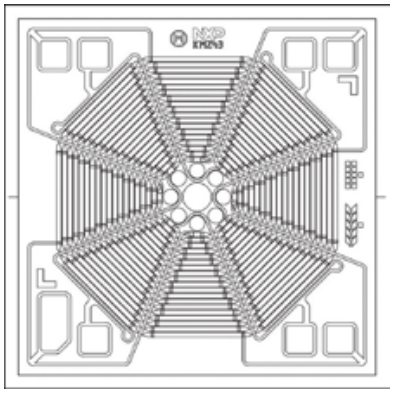

Figure 7.5: NXP KMZ43T chip layout, showing the 45°aligned bridges.

7.1.3 MultiPurpose Front-End for AMR sensors

NXP Semiconductors is the market leader in the field of AMR sensors and offers a wide portfolio of different products for angular speed and positioning measurement. Commercial examples are KMA220 dual channel programmable angle

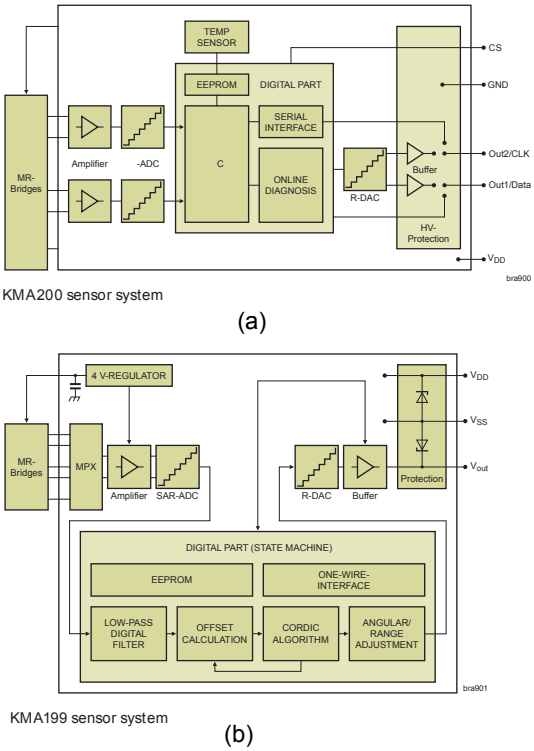

Figure 7.6: KMA200 (a) and KMA199 (b) sensor systems.

sensor [7.2], KMZ60 angle sensor with integrated amplifier [7.3] and KMZ49

magnetic field sensor [7.4]. The electronic interface differs in terms of architecture, performances and output signal (can be either a digital current or open collector).
Fig. 7.6 shows the architecture of the electronics in KMA200 (a) and KMA199 (b). As the interfaces are application specific, differences can be noted in the ADC converter and in the preamplification stage.
An analog Multi-Purpose Sensor Front-End (referred to as MPSFE) can be designed to serve as a general interface between application-specific magnetic sensors and application-specific digital part (Fig. 7.7), in order to ease and speed up the design of future sensor systems, as the analog flow is tipically costly and time consuming. Purpose of this project is the design of an application-

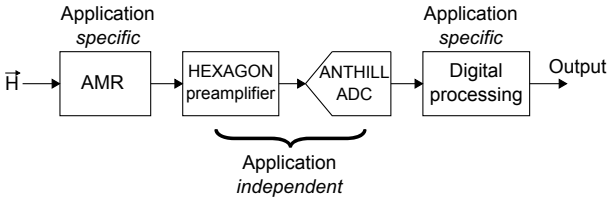

Figure 7.7: Sensor system with multi-purpose analog front-end.

independent preamplifier (referred to as HEXAGON) to be embedded in the Multi Purpose Sensor Front-End (MPSFE), in order to amplify the sensor output prior to the ADC conversion performed by the application independent $\Sigma\Delta$ converter ANTHILL. The target applications with the respective sensors are summarized in Tab. 7.1. The front-end specifications have been derived from the application specifications converting specifications like angle accuracy, maximum allowed angle error, output signal jitter (speed sensors), maximum rotational speed into front-end specifications like noise, offset, resolution, dynamic range, linearity, CMRR, PSRR, gain matching and so on. The resulting set of design specifications, together with the ANTHILL performance summary, has been used to design and correctly size the preamplifier discussed in this report. More details will be given in the following section.

	Speed	Angular
Application	ABS (OH503) Transmission Crankshaft	Steering BLDC Motors
Sensor	KMZ444	KMZE1

Table 7.1: Applications and related sensors.

7.2 Front-end specifications

The front-end specifications have been obtained collecting and processing data from the application specifications and converting them into electrical specifications. Fig. 7.8 summarizes the specification set obtained for the different applications. A complete set of desired performances for MPSFE, highlighted in the figure, has been derived taking the most strict constraint independently for each specification. The specifications reported have to be intended as maximum allowed values (at a 3σ confidence interval, where σ is the standard deviation). However, it should be pointed out that is not always necessary to satisfy every constraint at the same time. As an example, it is well known that small offset and large bandwidth are contrasting requirements, but the minimum front-end offset (13.75 µV) is required in case of steering application, which has the smallest bandwidth and signal frequency (2 kHz and 200 Hz, respectively). This kind of considerations enables the introduction of some degrees of programmability in the front-end design, or at least more flexibility, since apparently fighting specifications have not to be satisfied in every working condition. Using the measured ANTHILL performances it is possible to analyze the MPSFE specifications to derive the preamplifier desired performances. Another important constraint not mentioned in Fig. 7.8 is represented by the maximum silicon area: the preamplifier should not be larger than 0.1 mm^2 in a 3-channel configuration. It means that a single preamplifying channel should be smaller than 0.033 mm^2. This specification is clearly in contrast with the possibility of obtaining low offset and good gain matching with straightforward approaches, such as using large components to obtain good matching. Finally, the preamplifier will be designed using CMOS devices from the 0.14 µm 1.8 V ABCD9 SOI process, should be robust in the extended automotive range (-40°C to 200°C) over all the process corners and comply with the most severe level of DFM (Design for Manufacturability) rules (DFM3).

7.2.1 Gain and gain mismatch

The gain of the preamplifier is defined by the maximum input voltage divided by the maximum output voltage allowed by the specifications. The subsequent ADC ANTHILL has been designed to have an input peak differential voltage swing of 0.9 V. Then:

$$V_{out-max}/V_{in-max} = A_0 = \frac{0.9}{0.062} \approx 14.5 \tag{7.8}$$

	ABS	Transm.	Crank.	Steering	BLDC	MPSFE
Max. input voltage (mVp)	44.80	44.80	44.80	61.95	61.95	**61.95**
Bandwidth (kHz)	80.00	48.00	48.00	2.00	10.00	**80.00**
Max. sig. frequency (kHz)	20.00	12.00	12.00	0.20	1.00	**20.00**
DR (dB)	70.37	70.06	67.33	76.11	68.15	**76.11**
No. bits for noise (bits)	11.40	11.35	10.89	12.35	11.03	**12.35**
Noise level (nVrms/√Hz)	33.95	45.40	62.20	153.26	171.46	**33.95**
Linearity (bits)	6.76	6.76	6.76	12.14	10.49	**12.14**
Offset (uV)	414.41	414.41	414.41	13.75	42.97	**13.75**
Delay (us)	12.50	20.80	0.35	41.67	8.33	**0.35**
Chan. delay mismatch (ns)				1111.11	694.44	**694.44**
Chan. gain mismatch (dB)				57.10	47.20	**57.10**
CMRR (dB)	65.30	64.99	62.26	62.18	52.28	**65.30**
PSRR bridge supply (dB)	19.76	19.46	16.72	22.60	22.60	**22.60**
PSRR front-end (dB)	71.32	71.02	68.28	68.20	58.30	**71.32**
CM range (V)	0.66	0.66	0.66	0.67	0.67	**0.67**

Figure 7.8: Front-end specifications for different applications and MPSFE required performances.

However, to avoid amplifier saturation due to input DC offset, the gain A_0 has been set equal to 13. This point will be clarified in the following.
When dealing with angular sensors, the AMR sensor usually works in saturation conditions and only the direction of $\vec{H}$ is sensed, rather than its value. On the other hand, calculation of the angular speed in speed sensors relies only on counting zero-crossing events, whose frequency is not changed by gain variations. For these reasons, an absolute gain accuracy specification is not expressly given. However, since the gain influences front-end input noise and other performances, a maximum absolute gain error of 1% is desired. In case of angular sensors, it is necessary to achieve a very good gain matching between the preamplifier channel processing the sine and cosine components. Recalling what stated in Sec. 7.1.2, if a gain mismatch ΔA_0 is present, the output voltages V_{out1} and V_{out2} can be written as:

$$V_{out1} = A_0 \left(1 + \frac{\Delta A_0}{2}\right) \sin(2\alpha) V_{s1} \tag{7.9}$$

$$V_{out2} = A_0 \left(1 - \frac{\Delta A_0}{2}\right) \cos(2\alpha) V_{s2} \tag{7.10}$$

where α is the angle between $\vec{M}$ and the current I and $V_{s1,2}$ are the bridge outputs. It is clear that, due to the gain error, an error $\Delta\varphi$ comes out when the angle is calculated. Fig. 7.9 clarifies this concept, showing the angle error as a function of the angle 2α for a relative gain mismatch of 0.14% (Fig. 7.9a) and angle error as a function of gain mismatch itself (Fig. 7.9b). The chosen relative gain error (0.14%) is the maximum acceptable, corresponding to a maximum angle error equal to 0.8°. Considering a 3σ specification, the gain

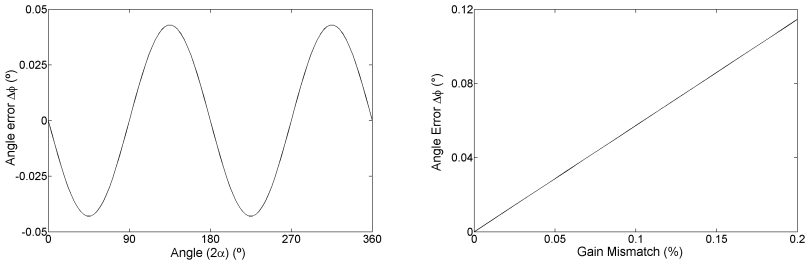

Figure 7.9: Effect of gain mismatch on angle calculations: angle error as a function of angle for a gain mismatch of 0.14% ((a)) and angle error as a function of gain mismatch (b).

mismatch specification $\sigma_{\Delta A_0/A_0}$ becomes:

$$\sigma_{\Delta A_0/A_0} \approx 0.05\% \tag{7.11}$$

This is also the strictest constraint given in Fig. 7.8, corresponding to the steering application. Such high gain-matching is not achievable with the allowed silicon area budget and requires the implementation of dynamic matching techniques.

7.2.2 Input noise and offset

Preamplifier noise budget

Front-end input referred noise and offset concur to define the system resolution. Input noise *rms* value gives the input Dynamic Range (DR) of the front-end, defined as:

$$DR = 20\log\frac{V_{max-rms}}{v_{n-rms}} = 20\log\frac{V_{max}}{\sqrt{2}v_{n-rms}} \tag{7.12}$$

where V_{max} is the maximum voltage at the bridge output and $V_{max-rms}$ its *rms* value and v_{n-rms} is the front-end input referred noise *rms* value. The noise and dynamic range specifications of the front-end for the different applications are shown in Fig. 7.8. They have been calculated taking into account the minimum angle to be resolved or the maximum allowed jitter on the output signal and the minimum signal amplitude expected from the sensor, considering also the thermal noise associated with the full-bridge resistors. If speed sensor applications are considered, noise budget is defined by the jitter on the output

square wave and is calculated as:

$$v_{n-rms} = \sqrt{\left(\frac{2\pi \cdot jit \cdot A_{min}}{100\sqrt{2}}\right)^2 - (v_{n-b})^2} \tag{7.13}$$

where jit is the percentage period rms jitter referred to signal frequency, A_{min} is the minimum sensor output signal amplitude (at maximum air-gap) and v_{n-b} is the bridge thermal noise, given by:

$$v_{n-b} = \sqrt{4kTR_b \cdot B} \tag{7.14}$$

where B is the signal bandwidth and R_b is the bridge resistance. For angular measurements, it can be shown that assuming equal noise contribution on both channels and considering the noise produced by two bridges, the front-end noise is calculated as:

$$v_{n-rms} = \frac{1}{\sqrt{2}}\sqrt{\left(A_{min}\alpha_n\frac{\pi}{180}\right)^2 - 2\,(v_{n-b})^2} \tag{7.15}$$

where α_n is the maximum allowed rms noise in the measurement of the angle. The factor $1/\sqrt{2}$ is due to the double channel configuration. Both the noise specifications have been calculated considering also temperature dependence of resistors and sensitivity. The sensor thermal noise power spectral density (PSD) $4kTR_b$ is proportional to absolute temperature T and is then maximum at the highest temperature (200°C). Thus, for a given total noise, the minimum front-end required noise is obtained at 200°C. This calculation has been performed for each application, obtaining the rms noise value. Then, considering the required bandwidth, the PSD can be calculated. The strictest noise constraint is obtained for the ABS application for $\alpha_n = 0.4°$, with v_{n_rms} equal to 9.6 µVrms at a temperature of 200°C, corresponding to a DR equal to 70.37 dB. The application bandwidth is equal to 80 kHz. Then, the noise PSD results to be equal to 33.95 nV/$\sqrt{\text{Hz}}$.

Considering the given specifications, the preamplifier gain A_0 and the measured performances of the ANTHILL ADC, and the following relationship, valid for thermal noise:

$$v_{n-rms}(T_2) = v_{n_rms}\sqrt{\frac{T_2}{T_1}} \tag{7.16}$$

it is possible to calculate the preamplifier thermal noise PSD at room temperature (27°C). The ADC measured dynamic range is equal to 14 bit (86 dB) at room temperature with 0.9 V maximum input, corresponding to an rms noise

of 32 µV. The measurement has been performed over a noise bandwidth of 20 kHz. The ADC noise PSD is then equal to 225 nV/$\sqrt{\text{Hz}}$ or to 17.35 nV/$\sqrt{\text{Hz}}$ if referred to the preamplifier input. Using Eq. (7.16), at room temperature the front-end noise PSD should be equal to 27 nV/$\sqrt{\text{Hz}}$. Then:

$$S_{v-pre} = \sqrt{\left(S_{v-FE}\right)^2 - \left(S_{v-ADC}\right)^2} = 20.7\text{nV}/\sqrt{\text{Hz}} \text{ at T} = 27°C \qquad (7.17)$$

where S_{v-pre}, S_{v-FE} and S_{v-ADC} are the input referred PSD of the preamplifier, front-end and ADC, respectively. This value is regarded as the noise requirement for the preamplifier.
It should be noted that until now only thermal noise has been taken into account. This because it is assumed that flicker noise is also removed when dynamic offset cancellation techniques are applied [7.5]. This will be clarified in the following.

Offset

The offset of the AMR is compensated over temperature in the digital domain or by trimming the AMR bridge. When no signal is present, the output of the front-end at room temperature is stored. Then, during operation, temperature is measured and an offset compensation algorithm computes the offset value at the actual temperature, assuming a linear ADC response, and then subtracts it from the front-end reading. This procedure is effective only if the front-end offset is negligible with respect to the AMR offset. When speed sensors are considered, the residual offset is given by:

$$V_{os-fe} = \min\left[\frac{V_{os-AMR}}{n}, A_{min}\sin\left(2\pi\frac{DDC}{100}\right)\right] \qquad (7.18)$$

where V_{os-fe} is the front-end offset, V_{os-AMR} is the AMR offset, A_{min} is the minimum voltage coming out from the bridge (at maximum air gap), DDC is the maximum duty-cycle error acceptable for the applications and n is an offset reduction factor, equal for instance to 3. The latter is specified in order to make the front-end offset negligible with respect to the AMR offset. Thus, the offset should be at the same time negligible with respect to the AMR offset and in any case small enough to meet the duty-cycle specifications.
On the other hand, when angular sensors are taken into account, an offset introduces an error on the angle calculation. To calculate this error, we can

consider that:

$$V_{s1} = A_{min} \sin(2\alpha) \pm V_{os-fe} \tag{7.19}$$

$$V_{s2} = A_{min} \cos(2\alpha) \pm V_{os-fe} \tag{7.20}$$

The $\pm$ is present because offset can be either positive or negative. Thus, 4 cases for different signs can be identified. Fig. 7.10 shows the angle error introduced by front-end offset in all cases, considering an A_{min} of 14 mV , V_{os-fe} equal to 13.75 µV. With these considerations in mind, front-end offset specifications

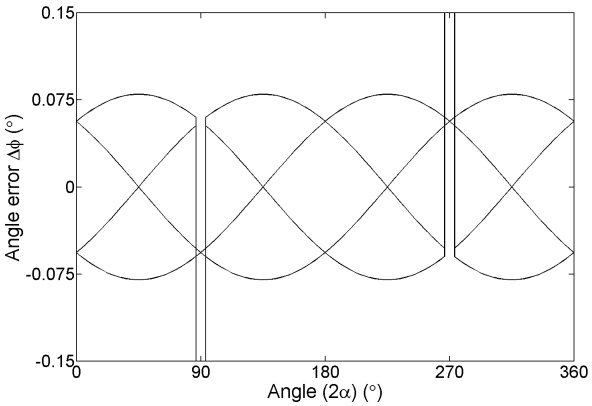

Figure 7.10: Angle error due to an offset of 13.75 µV on both channels.

have been derived and are reported in Fig. 7.8 for each application. The minimum offset level is 13.75 µV for the steering application. This value is determined by ADC offset and preamplifier offset. Since ADC offset is hard to minimize due to its architecture (switched capacitor $\Sigma\Delta$ with Correlated Double Sampling and high clock frequency, suffering from charge injection), the preamplifier offset should be minimized as much as possible. This specification is challenging, considering the minimum bandwidth requirement, equal to 80 kHz [7.5]. However, a preamplifier offset standard deviation σv_{os-pre} in the µV range, or, if not possible, at least lower than 10 µV should be achieved.

7.2.3 Linearity

Linearity of the front-end influences the way the AMR offset is corrected by the digital feed-forward compensation algorithm, leading to duty-cycle errors in speed sensors. Moreover, linearity clearly affects the angular accuracy. The required THD measured in bits is shown in Fig. 7.8 for each application. It ranges from 6.76 bits (corresponding to 42 dB) for speed applications to 12.14 bits (cor-

responding to 74.8 dB) for steering. Usually, trade-off between linearity and power consumption and thermal noise are found in CMOS circuits. However, analyzing the set of specifications, it can be observed that the strictest linearity constraint occurs for the maximum amplitude of the input signal (61.95 mV or even more, considering input offset), but for the lower bandwidth (2 kHz). This consideration will partially relax the linearity requirement, easing the design.

7.2.4 Output stage and driving capabilities

As cited above, the preamplifier is followed by the ADC ANTHILL. The latter is a switched capacitor 2^{nd} order 14 bit $\Sigma\Delta$ converter. It has 3 independent channels and for each channel the sampling frequency f_s is equal to 75 MHz. Such a high sampling frequency is necessary to cope with the jitter specifications. The input stage of the ADC is sketched in Fig. 7.11. Only one channel is represented. The working principle can be summarized as follows. The

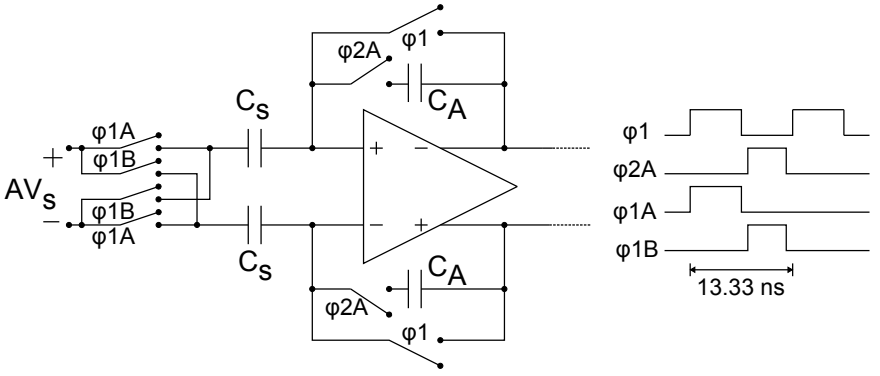

Figure 7.11: ADC input stage and phases. Only channel A is shown for simplicity.

sampling capacitors C_s, equal to 120 fF each, sample the preamplifier output voltage AV_s during phase φ_{1A}. During φ_{1B} the input switches invert the sign of the sampled voltage, in order to double the voltage swing on C_s and to maximize the charge transferred from C_s to the integrating capacitor C_A. The pulse duration $T_s/2$ of each phases is equal to 6.66 ns.

The differential sampled voltage should settle to AV_s when φ_{1A} is high and to $-AV_s$ when φ_{1B} is high. Fig. 7.12 represents the output stage of the preamplifier and the sampling capacitors of the ADC first stage, assuming that in the frequency range of interest Z_{out} is resistive. During the sampling phase, $V_c(t)$ is an exponential waveform, since we are dealing with a 1^{st} order system. The time constant τ is determined mainly by C_s and, if the on-resistance of the switches can be neglected, by the output impedance of the amplifier Z_{out}.

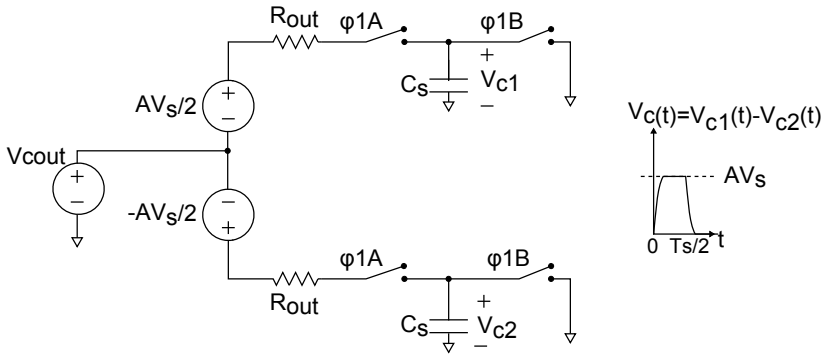

Figure 7.12: Simplified preamplifier output stage loaded with the ADC input S&H.

Assuming the resistive component of the latter still dominates at the sampling frequency (75 MHz), we have:

$$\tau = R_{out}C \tag{7.21}$$

where R_{out} is the value of the resistive component of Z_{out} at f_s. The voltage $V_c(t)$ during a sampling pulse can be written as:

$$V_c(t) = A\left(1 - e^{-\frac{t}{\tau}}\right) \tag{7.22}$$

Thus, at the end of a sampling pulse $T_s/2$ the settling error ϵ_s will be given by:

$$\epsilon_s = e^{-\frac{T_s}{2\tau}} \tag{7.23}$$

To avoid degrading ADC performances, this error should be lower than 1/2 LSB. With simple calculations a condition on R_{out} can be obtained:

$$R_{out} = \frac{T_s}{2C_s \ln(2^{15})} \tag{7.24}$$

With the given specifications, we obtain:

$$R_{out} \approx 5.35\ \text{k}\Omega \tag{7.25}$$

$$\frac{T_s}{2\tau} \approx 10.4 \tag{7.26}$$

The condition on R_{out} has to be intended as the value of Z_{out} at 75 MHz. This requirement is quite strict, because due to the output swing (0.9 V) and to the limited supply (1.8 V) source follower output stages are not practical. The adopted solution will be described later.

7.2.5 HEXAGON specifications summary

The main specifications of the preamplifier are summarized in Tab. 7.2. Be-

Specification	Value
Gain	13
Gain Mismatch (std)	**0.05 %**
Noise	$\approx$ 21nV/sqrtHz
Offset (std)	$\mathbf{< 5\ \mu V}$
THD	-42 dB to -75 dB
CMRR	65 dB
PSRR	72 dB
$\mathbf{R_{out}}$	$\mathbf{< 5.35\ k\Omega}$
Area (2-channels)	$\mathbf{0.066\ mm^2}$

Table 7.2: HEXAGON specification summary.

sides the above discussed specifications, the table reports also required CMRR and PSRR, as obtained from Fig. 7.8. The most challenging constraints are the gain-matching, to be achieved with a small silicon area, very low offset level with a moderate bandwidth, low output resistance, robustness to temperature and process, and linearity. It should be observed that no supply current constraints are given. Power consumption was not a primary concern in this design, since the aim of the project was to realize a proof of concept to test the implementation of techniques able to satisfy offset and gain-matching requirements, optimizing when possible the power without specified constraints.

7.3 HEXAGON architecture

7.3.1 Topology choice

In Chap. 3 the advantages of the current-feedback instrumentation amplifier over the standard 3-op-amp architecture have been discussed. Keeping in mind these previously discussed aspects, the current feedback topology has been adopted for the preamplifier design, especially because of the good trade-off between noise and power consumption and the possibility of easily implementing DEM techniques to increase accuracy reducing at the same time area occupation.

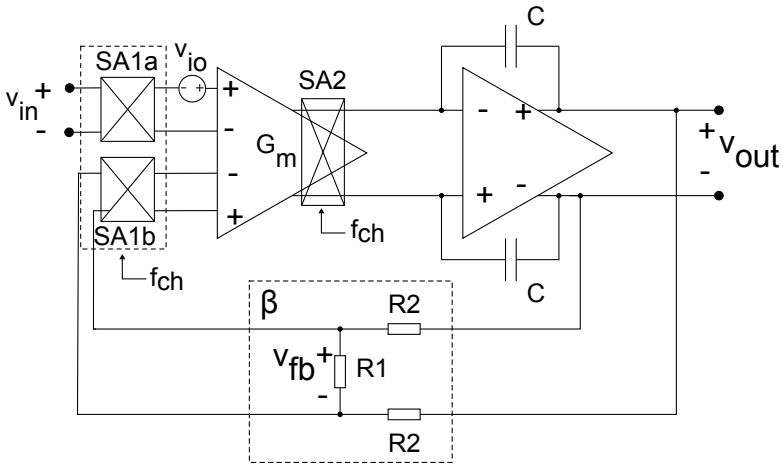

Figure 7.13: HEXAGON architecture.

7.3.2 HEXAGON topology

Principle of operation and chopper modulation

To achieve the required resolution over the given bandwidth (80 kHz) is then necessary to use dynamic offset cancellation (DOC) techniques [7.5], able to remove DC offset and strongly reduce flicker noise with only a limited impact on area occupation. Several examples of high performance CFIA using one or more DOC techniques have been previously discussed. However, they are generally characterized by a large area occupation, not acceptable for this design. Thus, traditional chopper modulation has been selected, due to its better trade-off between power consumption and base-band thermal noise PSD with respect to autozeroing.

Fig. 7.13 shows the Miller-compensated differential output chopper modulated current-feedback adopted architecture (same as Fig. 3.7). The frequency compensation is performed by C. It should be noted that g_{in} and g_{fb} are embedded into the double input port transconductor G_m. The equations describing the design of this topology have been given in Chap. 3 and in Chap. 4.

Again, we can indicate with g_{m-in} and g_{m-fb} the transconductance of input and feedback ports, respectively.

The gain A_d is given by:

$$A_d = \frac{v_{out}}{v_{in}} = \frac{g_{m-in}}{g_{m-fb}} \frac{1}{\beta} \tag{7.27}$$

where A_d is the amplifier DC gain. In ideal conditions, $g_{m-in} = g_{m-fb} = g_m$ and:

$$A_d = \frac{1}{\beta} = 1 + \frac{2R_2}{R_1} \tag{7.28}$$

Setting the gain A_d to 13, then $R_2 = 6R_1$ and $\beta = 1/13$. As extensively explained in Chap. 3 and 4, either a mismatch of the input transcoductances g_{m-in} and g_{m-fb} or of the resistive feedback network leads to a gain error, degrading the typical gain accuracy obtained from this architecture. Another source of error is represented by the finite loop gain. To achieve the required accuracy (0.05 %) with the given feedback factor (1/13), an open loop gain in excess of 90 dB has to be provided, pretty easy to achieve with the two stages structure. Chopper modulation has been applied to the instrumentation amplifier. Since a large bandwidth is required, multi-path topologies could be taken into account. However, the area requirement is very strict. For this reasons, the straightforward approach of increasing the chopper frequency has been chosen. This choice can lead to the increase of residual DC offset due to an increased charge injection and clock feedthrough contributions.

The modulated offset, often referred to as offset ripple, cannot be removed using a simple low-pass filter, since, given the low amplifier gain, the filter offset and noise performances would adversely impact the overall amplifier performances and increase significantly the required silicon area.

As explained in Chap. 3, output offset ripple, due to the integrating action performed by the Miller's capacitance, can have a triangular shape or a rectangular shape, depending on the relationship between f_p and f_{ch}. Increasing C in order to put f_p well under f_{ch} and reduce the ripple amplitude is not a viable approach, since this solution rapidly increases the area occupation. Alternative approaches to cope with the offset ripple have been proposed earlier, but are characterized by an increased area occupation and complexity and are not suitable for this design.

Generally speaking, the offset ripple rejection sets a lower limit on the circuit silicon area. However, if offset ripple amplitude is not as high as to significantly limit the output swing, filtering can be demanded to the digital part following the ADC. In our case, maximum signal amplitude is about 62 mV, while a maximum DC offset lower than 10 mV can be achieved in CMOS amplifiers with limited area impact. Thus, offset ripple can be tolerated and rejected in the digital domain. The main drawback of this approach is represented by the decrease of the gain (from 14.5 to 13, as described above), necessary to meet the requirement of 0.9 V maximum peak differential output. This only marginally

impacts the power consumption necessary to meet the noise performances of the system, contributing at the same time to a strong reduction of the circuit silicon area.

Dynamic Element Matching

In the previous section the main random sources of error affecting the gain accuracy of the amplifier have been pointed out:

- Mismatch of input transconductances g_{m-in} and g_{m-fb}
- Mismatch of feedback resistors

Defining as $\epsilon_{1,2}$ the gain errors affecting the channels and assuming they are uncorrelated and have the same standard deviation σ_ϵ, the normalized gain-mismatch $\Delta A_d/\overline{A_d}$ will have a standard deviation $\sigma_{\Delta A_d/\overline{A_d}}$:

$$\sigma_{\Delta A_d/\overline{A_d}} = \sqrt{2}\sigma_\epsilon \tag{7.29}$$

The specification reported in Tab. 7.2 is $\sigma_{\Delta A_d/\overline{A_d}} = 0.05\%$. This means $\sigma_\epsilon = 0.035\%$. Hypothesizing a perfect matching of g_{m-in} and g_{m-fb}, the gain error is determined by the feedback resistors mismatch. Fig. 7.14 shows the area budget necessary to obtain a 0.035 % mismatch of two p-poly resistors with R = 10 kΩ. The mismatch model has been obtained from the CMOS14 process manual. To meet the mismatch specification, a silicon area of $2 \cdot 10^4$ µm^2 is

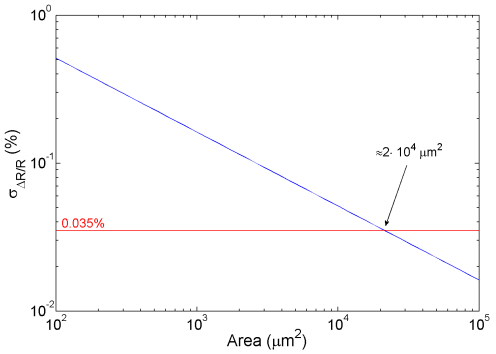

Figure 7.14: Mismatch standard deviation $\sigma_{\Delta R/R}$ versus silicon area. Resistors are p-poly type, with R=10 kΩ.

required. With the given sheet resistance $R_{sh} = 107.5$ Ω, the resistor width W results to be equal to 10 µm. These values are not acceptable, since the HEXAGON area budget does not allow such large passives to be integrated. A possible solution to obtain a very accurate absolute gain is described in [7.6]. It

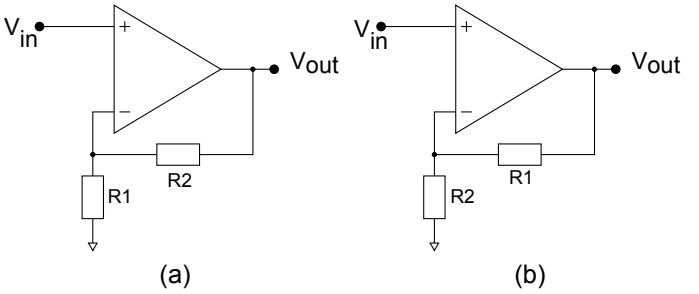

Figure 7.15: Principle of operation of the DEM technique proposed in [7.6]. In (a) the resistor placement during the first phase is shown, in (b) during the second phase.

consists in using dynamic element matching of the feedback network in order to cancel the mismatch error without using trimming techniques. Fig. 7.15 shows the principle of operations. The resistors R_1 and R_2 are equal by design and are exchanged over a clock cycle. During the first phase they are placed as in Fig. 7.15(a) and the gain is given by:

$$G_1 = 1 + \frac{R_2}{R_1} \tag{7.30}$$

During the second phase (Fig. 7.15(b)), the gain is given by:

$$G_2 = 1 + \frac{R_1}{R_2} \tag{7.31}$$

If $R_1 = R_0(1 + \Delta R)$ and $R_2 = R_0(1 - \Delta R)$, the average gain over two clock cycles becomes [7.6]:

$$\overline{G} = 1 + \frac{1 + \Delta R^2}{1 - \Delta R^2} \approx 2(1 + \Delta R^2) \tag{7.32}$$

if $\Delta R << 1$. The resistor mismatch is then reduced to a second order effect. A 1% error results after DEM into a 0.01% mismatch. To set a gain equal to N, N resistors are necessary, which need to be shifted along all possible positions into the network. The implementation of the feedback network of the described CFIA amplifier is shown in Fig. 7.16. The switches are necessary to implement the required connections. Unfortunately, traditional MOS switches suffer from non-linearity introduced by the on-resistance dependency on the source voltage and by the body effect. To avoid a THD degradation, it is necessary to keep them out of the transfer function. This is achieved taking the output at the nodes V_{u+} and V_{u-}, as shown in the figure, instead of V_{out+} and V_{out-}. By this way, if the stage following the preamplifier has an high input impedance,

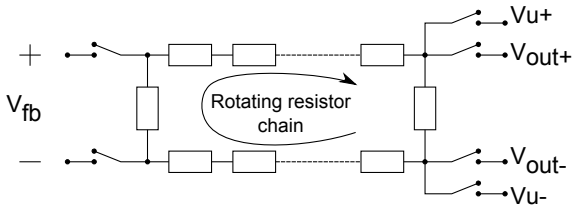

Figure 7.16: DEM implementation of the feedback network.

no current flows through the additional switches and they do not appear into the transfer function and for this reason do not introduce nonlinearities.
The gain error due to mismatch can be written [7.6]:

$$\epsilon = \frac{1}{N}\sum_{i=1}^{N}\Delta R_i^2 \tag{7.33}$$

and can be estimated as $\Delta R^2/\sqrt{N}$.
This approach is very effective in cancelling out the gain error introduced by the resistors, decisively decreasing the required area. However, 6 switches are necessary for each node of the resistor chain. In our case, this results into 84 MOS switches. As a large voltage swing is applied to the switches, it is necessary to implement them as pass-gate, with a large W not to increase their on-resistance. In addition, a gain ripple is originated, due to the DEM technique. The ripple period depends on the frequency the chain is rotated at. This ripple has also to be filtered. The minimum ripple frequency is then set by the bandwidth requirement of the amplifier (80 kHz). Thus, the minimum DEM clock frequency results to be around 1.4 MHz, since 14 different positions of the chain are possible. The size of the switches, combined with the high DEM frequency, could easily result into an increased offset due to charge injection. An alternative approach, consisting in modulating this injection with additional chopper modulators, has been evaluated. Fig. 7.17 shows the resulting architecture. Modulator SA1b has been introduced. In this way, DC offset contribution due to DEM switches charge injection is removed by SA2, since the spikes have always the same polarity. Moreover, SA1b can be implemented properly driving the DEM network switches.
Although an implemented proof of concept has shown the feasibility of this technique, the large number of switches and connections, together with the digital logic required to correctly drive them, turned into increased circuit and layout complexity, making this approach not practical and not so efficient in terms of area saving.

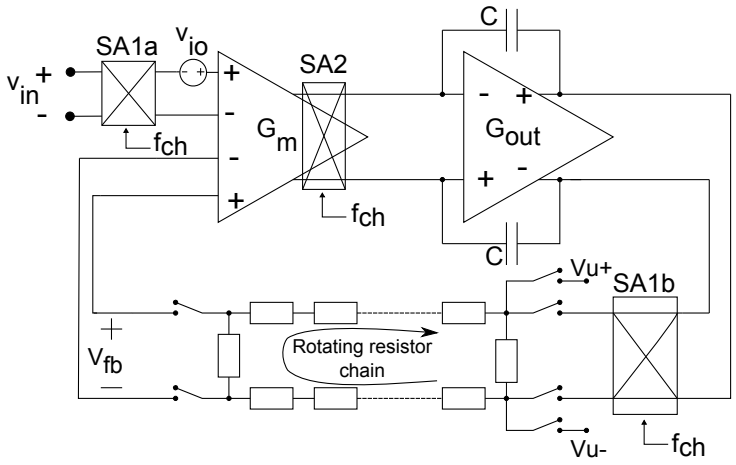

Figure 7.17: Architecture of the preamplifier with dynamic matching of the feedback network and chopping to remove charge injection.

The resistor mismatch seems then to put a limit on the absolute gain accuracy achievable with simple solutions. However, it should be noted than an absolute high gain accuracy on a single-channel is not required, as described in the previous section. Both channels can have a significant gain spread but at the same time have a very good gain matching. This can be achieved performing dynamic matching between the two channels, instead of on each channel separately. Hypothesizing that the first channel has a gain $G_1 = G_0(1 + \Delta G)$, due to random errors, and the second channel has a gain $G_2 = G_0(1 - \Delta G)$, it is possible to exchange the source of errors, i.e. the feedback network if transconductors perfectly match, between the two channels. In this way, over a DEM period we obtain an average gain $\overline{G}$ for each channel:

$$\overline{G} = \frac{G_1 + G_2}{2} = G_0 \tag{7.34}$$

The mismatch between the channels is thus completely cancelled out averaging over a DEM period, rather than only reduced to a second order effect. A practical implementation of the dynamic feedback network matching between the two channels is shown in Fig. 7.18. Feedback networks β_1 and β_2 are exchanged between the two channels by modulator SA-D1, which connects the outputs of each channel to one resistive divider or to the other, depending on the phases ϕ_{D1} or ϕ_{D2}, respectively. The modulator SA-D2 is necessary to correctly close the feedback.

The switches of SA-D1 directly influences the linearity of the amplifier. If

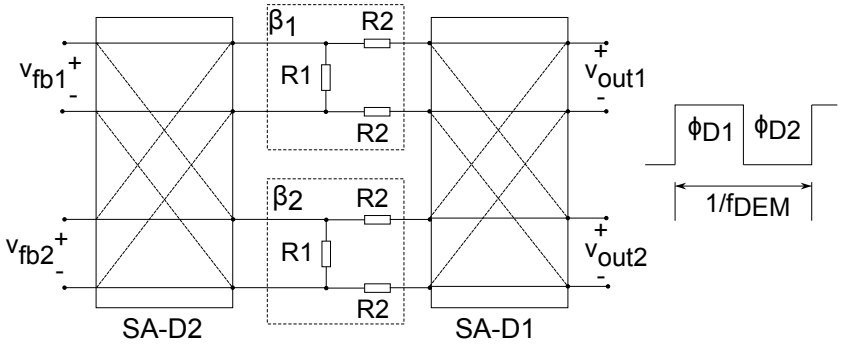

Figure 7.18: Implementation of dynamic feedback network matching between the two channels.

implemented with simple MOS switches, the on-resistance r_{on} is given by:

$$r_{on} = \frac{1}{k\,(V_{gs} - V_{TH})} = \frac{1}{k\,(V_{ck} - V_s - V_{TH})} \tag{7.35}$$

where V_{ck} is the clock voltage, $k = \mu C_{ox} W/L$ and V_s is the source voltage. The resistance r_{on} varies with V_s. Since those switches are positioned at the amplifier output, they experience large source voltage variations. Although their r_{on} can be made small with respect to the feedback resistors, the harmonic distortion introduced is still significant. To solve this issue, switches of SA-D1 have been implemented as bootstrapped switches, in order to keep r_{on} constant when the output voltage changes by keeping $V_{GS} = V_{dd}$. Moreover, the on-resistances of SA-D1 switches are not exchanged between the two channels, but are in series with R_2. For this reason, they have to be negligible with respect to the latter, in order to introduce a small enough gain-mismatch. The design of the switches will be presented in the next section.

Up to this point, the gain error introduced by the transconductances mismatch has not been taken into account. To come over this issue, a possible solution is to implement the Dynamic Element Matching of the input transconductors described in Chap. 4. With this technique, the relative gain error is reduced from $\Delta g_m/g_m$ to Δg_m^2. For a transconductance mismatch of 1-5%, this technique reduces the gain error to 0.01%-0.25%. Considering the gain-mismatch dependent only on the transconductance mismatch, the maximum mismatch $\Delta g_m/g_m$ of each channel should be, accordingly to Eq. 4.37, 1.22% to obtain a gain error of 0.035%. This value is still not straightforward as it requires a very good matching of the differential pairs and of the tail current sources. Moreover, g_{m-in} and g_{m-fb} are also dependent on the common-mode voltage applied to its input, although to a second order. This dependence can still limit

the accuracy of the CFIA gain, if input and output common mode voltages are different. The gain error ϵ_{cm} has been shown in [7.7] and is reported here:

$$\epsilon_{cm} \approx \frac{\Delta g_m \Delta \text{cm}}{2} + \Delta \text{cm} \tag{7.36}$$

where Δcm is the extra mismatch due to the different CM level of g_{m-in} and g_{m-fb}. This term is not canceled by the DEM technique. Although the g_m modulation introduced by a CM voltage variation is usually a second order effect, a CM difference between signal and feedback paths of a few tens of mV can introduce a gain mismatch in the range 0.01-0.1%, depending on the transconductor CMRR and is therefore not negligible in this application. In [7.7] a partial solution is provided, consisting in increasing the differential pair CMRR.

This DEM technique contributes to improve the gain-matching, since it improves the gain error spread of each channel, but a good transconductor matching is still necessary. To achieve a very good gain-matching between the two channels without imposing specifications on the gain spread of a single channel, it is possible, as in the case of the feedback network, to operate a dynamic matching of the first stage between the two channels. Fig. 7.19 shows the principle of operation of the proposed technique. It basically consists in exchanging the first stages between the two channels over a DEM cycle. The entire channels cannot be exchanged. This because the second stage has memory, due to the Miller's capacitors and an exchange of the two channels would result in an high crosstalk. Chopper modulation phases $\phi_{1,2}$ have period $1/f_{ch}$ and DEM phases $\phi_{3,4}$ have period $1/f_{DEM} = 1/2f_{ch}$. DEM phases have to be at least a multiple of 2 times longer than chopper phases to allow the offset compensation of each channel to be performed. This will be clarified in the followings. Chopper modulation and DEM can be implemented with a single input modulator, SA-Din, using d1-d4 phases. To properly understand how the technique works, the circuit configuration during each of the d1-d4 phases is described:

- **phase d1:** inputs v_{in1} and v_{in2} are connected in a straight fashion to G_{m1} and G_{m2}, respectively, by SA-Din. Modulators SA1b1 and SA1b2 connect the feedback voltages to the feedback ports with no sign inversion. SA21 and SA22 also do not perform sign inversion. SA-Do connects straightly the outputs of the first stages to the second stages, not represented in figure.

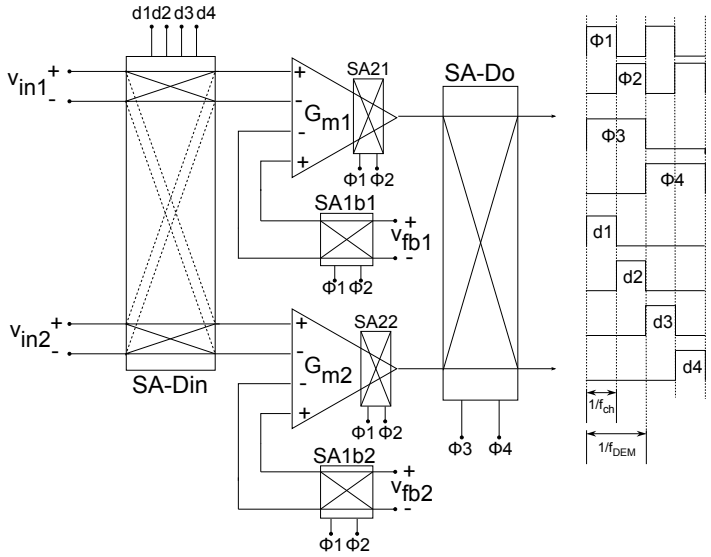

Figure 7.19: First stage dynamic matching architecture with phases.

- **phase d2:** inputs v_{in1} and v_{in2} are now connected in a crossed fashion to G_{m1} and G_{m2}, respectively, by SA-Din, which thus performs only sign inversion. Modulators SA1b1, SA1b2 also perform sign inversion to maintain the negative sign of the feedback. On the other hand, SA21 and SA22 perform sign inversion to shift the offset of G_{m1} and G_{m2} at higher frequencies (around f_{ch}), thus implementing chopper modulation. Outputs of the first stage are still straightly connected.

- **phase d3:** inputs v_{in1} and v_{in2} are now straightly connected to G_{m2} and G_{m1}, respectively, with no sign inversion. Modulators SA1b1 and SA1b2 connect the feedback voltages to the feedback ports with no sign inversion. SA21 and SA22 also do not perform sign inversion. SA-Do now connects the outputs of G_{m1} to the second stage of channel 2 and G_{m2} to the second stage of channel 1, not represented in figure.

- **phase d4:** inputs v_{in1} and v_{in2} are now connected to G_{m2} and G_{m1}, respectively, with sign inversion. Modulators SA1b1, SA1b2 also perform sign inversion to maintain the negative sign of the feedback. Again, SA21 and SA22 perform sign inversion to implement offset modulation. This is necessary to compensate for the offset contribution of the exchanged transconductors during d3-d4 (phase $\phi 4$). SA-Do still connects the outputs of G_{m1} to the second stage of channel 2 and G_{m2} to the second stage of channel 1.

By this way, input transconductors G_{m1} and G_{m2} are alternatively connected to v_{in1} and v_{in2} and DEM is implemented. All the gain errors related to the first stage can then be cancelled out by averaging over a DEM period. It should be also observed that an additional ripple is originated, in addition to the offset ripple, at f_{DEM} frequency. Also this ripple can be filtered out in the digital domain. As an example, with a worst case gain-mismatch of 5%, a gain of 13 and an input voltage of 50 mV and $f_{DEM} < f_p$, the gain ripple appearing at the output will have a peak-to-peak amplitude of 32.5 mV.
As stated above, since v_{fb1} and v_{fb2} are always connected to the same transconductor, while the inputs are exchanged, modulator SA-D1, shown in Fig. 7.18, is not necessary.
With the proposed dynamic matching techniques the main sources of error are compensated and a very low gain-mismatch can then be expected. However, the difference of input and output common mode voltages and its mismatch still introduces a gain-mismatch. This aspect will be discussed in the following section.

7.3.3 Common-mode feedback

The fully-differential architecture requires a common-mode feedback (CMFB) to set the common-mode output voltage. If G_{out} has a common-mode gain, it is possible to stabilize the output common-mode voltage acting only on G_m. The architecture of the preamplifier including the common-mode loop is shown in Fig. 7.20. The output common-mode V_{cmo} is sensed by the feedback resistive divider, with R_1 split into two resistors of value $R_1/2$. Amplifier A_{CM} senses the difference between V_{cmo} and a voltage reference V_{ref} and drives G_m in order to move V_{cmo} towards the reference value, thanks to the negative feedback.
The output common mode voltage is 0.9 V by design, as the input common-mode voltage. In this ideal case, the CM-related gain error discussed in the previous section is not present. However, some non-idealities are present and have to be taken into account: the voltage source V_{o-cm} represents A_{cm} input offset. Moreover, due to the limited loop gain of the CMFB, V_{cmo} results to be different from V_{ref}. Finally, since V_{ref} is usually obtained with simple resistive dividers from the supply voltage, it has a spread. Due to these factors, a spread of the output common mode voltage in the order of around 10-20 mV can be expected, different for the two channels. According to Eq. 7.36, this will translate into an unacceptable gain-mismatch in the order of 0.05-0.1%. The architecture shown in Fig. 7.20 solves this issue. Actually, thanks

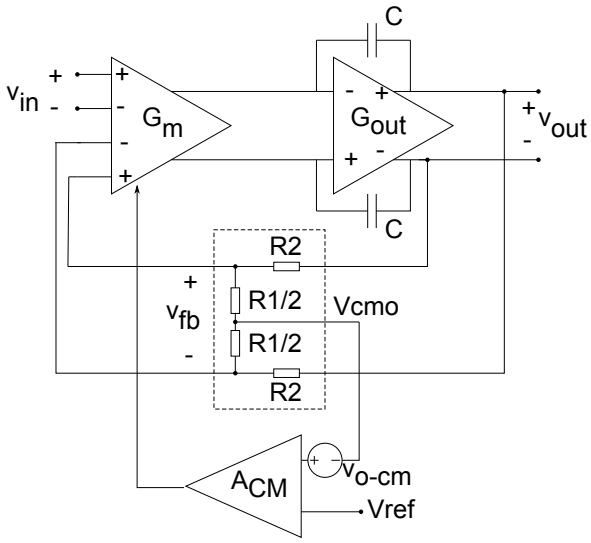

Figure 7.20: Preamplifier architecture with common-mode feedback loop.

to the exchange of the feedback networks and first stages shown in Figs. 7.18 and 7.19, the CMFB circuits are swapped between the two channels and the gain-mismatch they introduce is modulated by the DEM technique and can be averaged out.

Fig. 7.21 shows the complete architecture of the 2-channels preamplifier.

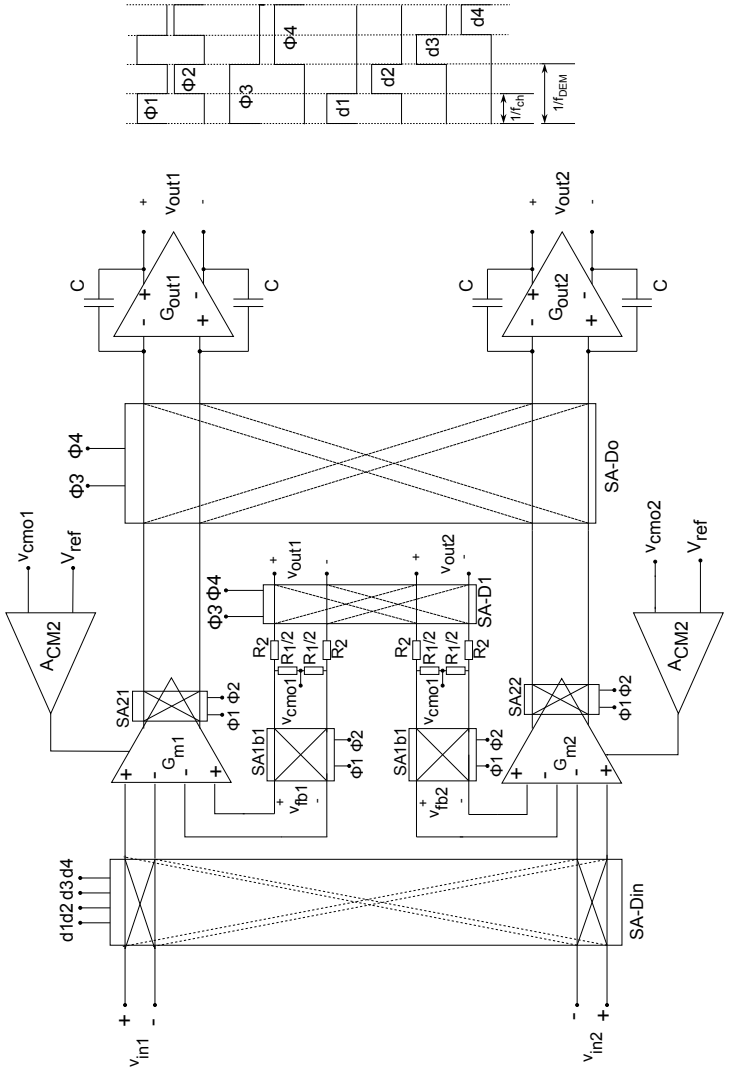

Figure 7.21: HEXAGON architecture.

7.4 Circuit design

The circuit has been designed in order to meet the specifications previously discussed and to be robust against large process and temperature variations. In addition, since in this test-chip the ADC is not present, the preamplifier has to drive the output pads. For this reason, stability with a load capacitance of 100 pF on each output terminal has been ensured.

7.4.1 Noise analysis

The tight specification requires a low-noise targeted design. To understand how the noise of single blocks contributes to the total input noise PSD, it is possible to make reference to Fig. 7.22. A single channel is shown, since the noise specification is referred to the single-channel amplifier. Noise voltage sources are also shown. The voltage source v_{n1} represents the input noise of

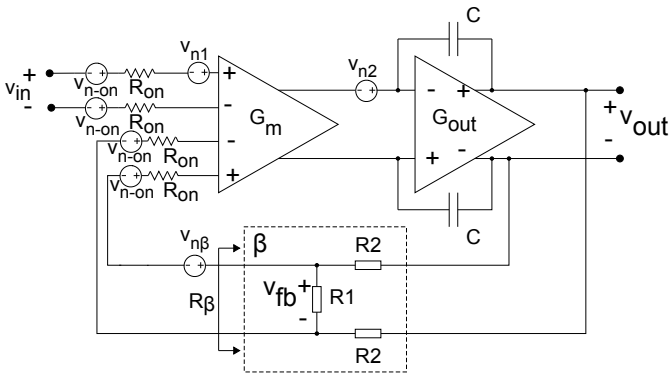

Figure 7.22: Single-channel preamplifier with noise sources.

the first stage G_m, v_{n2} input noise of G_{out}, v_{n-on} the noise of the switches on-resistance R_{on} and $v_{n\beta}$ the noise introduced by the feedback resistors. The resistance R_β is the resistance seen looking into the feedback network from the input, and is:

$$R_\beta = R_1 // 2R_2 \approx R_1 \tag{7.37}$$

The input voltage noise PSD can then be written as:

$$S_{v-in} = S_{n1} + 4S_{n-on} + S_\beta + \frac{S_{n2}}{A_1^2} \tag{7.38}$$

where S_{n1} is the PSD of v_{n1}, S_{n2} the PSD of v_{n2}, S_{n-on} of v_{n-on}, S_β of $v_{n\beta}$ and A_1 is the voltage gain of G_m. Since A_1 is usually large to achieve an high

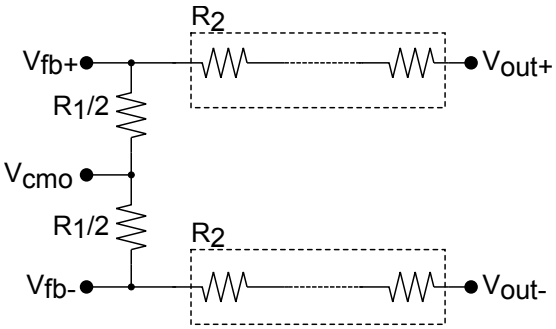

Figure 7.23: Resistive feeback network.

enough loop gain, S_{n2} is negligible. We have:

$$S_{n-on}^2 = 4kTR_{on} \tag{7.39}$$

$$S_\beta^2 = 4kTR_\beta \tag{7.40}$$

Since chopper modulation is used, the contribution of G_m to the input noise PSD is given by $S_{n1}(f)$ evaluated at f_{ch}. Since f_{ch} is 200 kHz, the contribution is mainly thermal.

7.4.2 Feedback network

Resistive feedback network has been designed using n-Poly resistors. It is shown in Fig. 7.23. Resistors R_2 have been realized with 12 series resistors of value $R_1/2$ each. As an acceptable compromise between current flowing through $R_1 + 2R_2$ and input noise PSD contribution, R_1 has been made 4 kΩ and R_2 results then equal to 24 kΩ. Then:

$$S_\beta^2 = 4kTR_\beta \approx 4kTR_1 = 66.2 \cdot 10^{-18}\ \mathrm{V^2/Hz} \tag{7.41}$$

corresponding to 8.1 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. When $V_{out} = 0.9$ V, current flowing through the network is 17.3 µA. To limit DEM related gain ripple amplitude, the resistors have been sized 1 µm wide and 17 µm long, in order to decrease β spread.

7.4.3 Switches design

The modulators used in the amplifier are all implemented by means of MOS switches. Wherever possible, nMOS switches have been used, to decrease switch on-resistance R_{on}.
With the phase choices depicted in Fig. 7.21, each modulator can be build

avoiding the use of more than one series switch for each path. Since the input common mode voltage is 0.9 V, input modulator SA-Din has been built with nMOS switches. Also SA1b1 modulators have been built with nMOS switches, since they experience a small voltage variation around the output common mode, approximately equal to 0.9 V, just as SA-Din. Modulator SA-D1 has been implemented using bootstrapped nMOS switches. Schematic of the latter will be shown later. Modulators SA21-SA22 are embedded into the G_m stage and their design will be shown in the section describing the transconductor. Finally, modulator SA-Do has been built using minimum size switches (0.768x0.16 μm^2). As it will be clarified later, $G_{m1,2}$ have four outputs each, two with low common-mode voltage and two with high common-mode voltage. Then, each switch in SA-Do has to be implemented with either a nMOS or a pMOS switch depending on their position.

As widely discussed above, input switch sizing is critical. Using process parameters and the equations given in Chap. 2, the offset contribution of a minimum-size nMOS switch pair can be estimated. The clock swing is 1.8 V, $W = 0.768$ µm , $L = 0.16$ µm, $C_{ox} = 12$ fF/μm^2, $\sigma_{VTH} = 15$ mV, $C_{ov} = 200$ aF. Assuming a source voltage of 0.9 V, we have $V_{GS} - V_{TH} = 0.35$ V. For the other parameters spread, we assume $\sigma_{\Delta W/W} = \sigma_{\Delta L/L} = \sigma_{\Delta C_{ov}/C_{ov}} = 5\%$. Switch R_{on} resistance is 2.3 kΩ and R_s is 5 kΩ (bridge resistance).

With the given values we obtain for the switch pair an offset contribution $\sigma_{Vos} = 0.5$ µV with $f_{ch} = 200$ kHz. This estimation generally leads to underestimation of the residual offset. The latter roughly increases with $\sqrt{W}$, since channel charge and C_{ov} both increase with W, while mismatch decreases with $\sqrt{W}$. On the other hand, thermal noise PSD introduced by a pair of minimum size nMOS switches is $\sqrt{2 \cdot 4kTR_{on}} = 8.7$ nV/$\sqrt{\text{Hz}}$. Since two pairs of input switches are always on, the total switches noise contribution is 12.3 nV/$\sqrt{\text{Hz}}$, which is relatively high, if compared with the total noise target (21 nV/$\sqrt{\text{Hz}}$). In addition, Spectre noise simulations show a thermal noise level associated with a nMOS minimum size switch pair of about 9.7 nV/$\sqrt{\text{Hz}}$, corresponding to an increase of 11% with respect to the value (8.7 nV/$\sqrt{\text{Hz}}$) predicted by Eq. (7.40). Then, for two switch pairs, we have a total noise contribution of 13.67 nV/$\sqrt{\text{Hz}}$ and an offset contribution (σ) of 0.7 µV. However, increasing switches width in order to decrease their R_{on} would in turn increase the residual DC offset. For this reason, minimum size switches have been used.

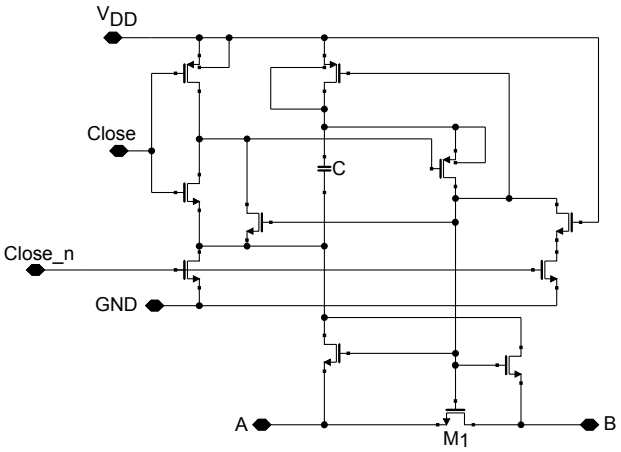

Figure 7.24: Bootstrapped switch used in SA-D1 modulator.

Bootstrapped switch design

Modulator SA-D1, necessary to implement feedback network DEM, experiences the full-swing output voltage V_{out} at its input. Simple nMOS switches are not able to handle such a large voltage swing. Pass-gates could be employed. However, their on-resistance is strongly dependent on the source voltage, which in this case is the output voltage. Due to this, THD would result to be degraded, since the gain also depends on the SA-D1 switches on-resistance.
To preserve linearity, bootstrapped nMOS switches have been used. With this topology, it is possible to drive the switch with a fixed V_{GS} voltage, which does not vary with the source voltage. The adopted switches are shown in Fig. 7.24. The actual nMOS switch is M_1. It has $W = 10$ µm and minimum L (0.16 µm). Since the gate-source voltage is maintained at 1.8 V when Close is high, its on-resistance R_{on-b} is about 68.4 Ω. To make the circuit robust to leakage, C is 2 pF.
Since M_1 is in series with R_2, it is important to evaluate how much it impacts on the gain, which results:

$$A_d = \frac{1}{\beta'} = 1 + \frac{2R_2 + R_1 + 2R_{on-b}}{R_1} \approx 13.034 \tag{7.42}$$

The relative error introduced on the absolute gain by the switch is about 0.26 %. The gain-mismatch introduced by the switches mismatch is not processed by DEM, since two switch pairs for each channel are swapped each DEM phase. Then, the gain spread introduced on each channel will be given by $\sigma_{\Delta ron-b/ron-b}/\sqrt{2}$. When the gain-mismatch between two channels is consid-

ered, a multiplying factor $\sqrt{2}$ has to be considered. Then, the relative gain-mismatch standard deviation induced by the DEM switches can be simply estimated as $\sigma_{\Delta ron-b/ron-b}$. The latter is given by:

$$\sigma^2_{\Delta ron-b/ron-b} = \sigma^2_{\Delta\beta/\beta} + \frac{\sigma^2_{\Delta V_{TH}}}{(V_{GS} - V_{TH})^2} \tag{7.43}$$

Since $(V_{GS} - V_{TH}) = 1.36$V and the nMOS is not minimum, the mismatch is dominated by $\sigma_{\Delta\beta/\beta}$. MonteCarlo simulations performed with Spectre returned $\sigma_{\Delta ron-b/ron-b} \approx 0.6\%$. Considering the gain error introduced by the switches and their mismatch, a residual gain-mismatch with $\sigma \approx 0.016\%$ can be estimated, which is considerably lower than the specification ($\sigma_{\Delta A_d/A_d} = 0.05\%$).

7.4.4 Input stage

The input stage design is critical, since input transconductors contribute to define important preamplifier performances such as input noise PSD and linearity. It should also be robust against process and temperature variations.
The first stage noise budget can be calculated and results to be 13.7 nV/$\sqrt{\text{Hz}}$.
The adopted topology is shown in Fig. 7.25. It is a folded-cascode gain-boosted

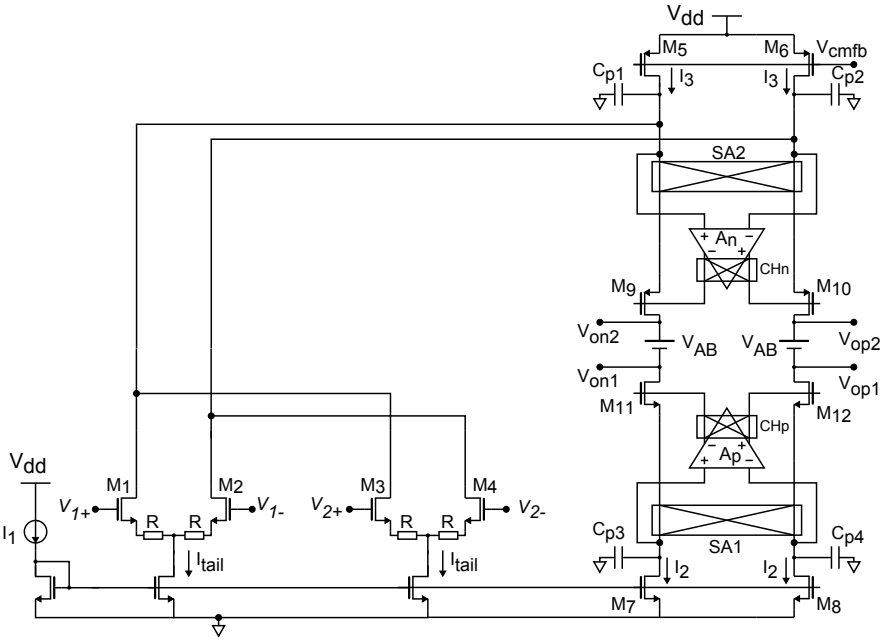

Figure 7.25: First stage topology.

amplifier employing source degeneration to increase the input range, with embededded chopper demodulators SA1 and SA2. It also includes floating batteries for second-stage class AB biasing. Gain-boosting is performed by folded-cascode amplifier A_n and A_p. The former has nMOS input stage and the latter pMOS input stage, to comply with the input voltage level. Stability of the boosting loop has been ensured adding capacitance of 0.35 pF and 0.45 pF at the output of A_n and A_p, respectively.
Differential pair tail current I_{tail} has been set to 80 µA, the cascode branches have been biased with $I_2 = 10$ µA and, as a consequence, current sources M_5 and M_6 has to provide a current of 90 µA each. Transistors M_9-M_{12} cascode the current sources. Offset current of M_5,M_6 and M_7,M_8 are also modulated by SA2 and SA1, respectively.
Input devices have been biased in weak inversion region to maximize g_m/I_d ratio for low noise operation and made large enough (80 µm/0.85 µm) to make negligible their flicker contribution at f_{ch}. The M_1-M_4 g_m is then 860 µS. The linear input range has been extended using degeneration resistors $R = 550\ \Omega$. The input stage transconductance G_m results then to be given by:

$$G_m = \frac{g_m}{1 + g_m R} \approx 580\ ^{-}\text{S} \tag{7.44}$$

However, simulated G_m is about 549 µS. DC gain is 138 dB, gain-bandwidth product (GBW) with 5 pF load on each output is 17.25 MHz.
Input noise PSD is given by:

$$S_{v-in} = 4S_{vR} + 4S_{v1} + 2\frac{S_{I5}}{G_m^2} + 2\frac{S_{I7}}{G_m^2} \tag{7.45}$$

where S_{vR} is the degeneration resistor thermal noise voltage PSD, S_{v1} the gate-referred noise voltage PSD of M_1-M_4, S_{I5} the noise current PSD of M_5 and M_6 and S_{I7} the noise current PSD of M_7 and M_8. Noise simulations report noise PSD of 14.8 nV/$\sqrt{\text{Hz}}$ at f_{ch} with $T = 27°$C and a corner frequency f_k of 62 kHz, well below $f_{ch} = 200$ kHz. In this way, most of the flicker noise contribution is rejected thanks to chopper modulation. It should be noted that the achieved input noise PSD is slightly larger than the initially allowed noise budget (13.7 nV/$\sqrt{\text{Hz}}$). This is mainly due to the challenging requirement of robustness against process spread and temperature range (-40 to 200 °C), which restricted the freedom in choosing the biasing of the transitors. Moreover, the flicker contribution of M_5 and M_6 at f_{ch} can be made negligible increasing their area. This cannot be made at will. Actually, the C_{gs5} introduces a pole in the

common-mode loop driving M_5 and M_6 gates, which can degrade stability. For these reasons, a slightly larger noise level has been traded mainly for stability and robustness and considered acceptable.
Total noise contribution of M_5, M_6 is 34.7%. Differential pairs contribute with 34.5% of total noise. Degeneration resistors also give a contribute of around 24%. Noise contribution of M_7 and M_8 is only 5.4%. Total flicker noise contribution at 200 kHz is lower than 24%.
It is interesting to calculate the lowest current necessary to meet the noise specification if only the differential pairs, without source degeneration, contribute to the input noise PSD, in order to understand how much the power consumption had to be increased for linearity, robustness and stability. To minimize gate-referred voltage noise PSD, the transistors should work in sub-threshold region. The current PSD results then to be given by:

$$S_{I-w}^2 = 2qI_d \tag{7.46}$$

where I_d is the drain current. The transistor g_m in this region is:

$$g_m = \frac{I_d}{nV_T} \tag{7.47}$$

where $n \approx 1.4$ for bulk CMOS processes and is slightly lower (≈ 1.3) for SOI-CMOS processes and $V_T = kT/q = 26$ mV at 27°C. Then, gate-referred noise PSD is:

$$S_{vg-w}^2 = \frac{S_{I-w}^2}{g_m^2} = \frac{2qI_d n^2 V_T^2}{I_d^2} = 2n^2 kT \frac{V_T}{I_d} \tag{7.48}$$

To meet the desired specification (13.7 nV/$\sqrt{\text{Hz}}$), it should hold:

$$S_{v-in}^2 = 4S_{vg-w}^2 = 187.7 \text{ V}^2/\text{Hz} \tag{7.49}$$

Then, $S_{vg-w}^2 = 46.9$ V^2/Hz, corresponding to 6.85 nV/$\sqrt{\text{Hz}}$. Considering $n = 1.3$, we obtain the minimum value $I_d = 7.7$ µA. It should be observed that this value is much lower than $I_{tail}/2$, but this calculation has been made considering deep sub-threshold, simple differential pairs and neglecting the noise contribution of other devices.
Residual offset contributions introduced by the modulators can be analyzed. Modulators SA2 and SA1 suffer from charge injection and clock feedthrough mismatch, similar to what happens for the input switches. Due to this, a current spike will appear at the transconductor output, corresponding to an input voltage spike, which can be translated into a DC offset, since these spikes are

demodulated by the input modulators. The contribution to the input offset voltage is given by:

$$\sigma_{Vos} = \frac{\sigma_{q-t} f_{ch}}{G_m} \tag{7.50}$$

where σ_{q-t} is the total charge mismatch and G_m is the transconductance of the first stage. The charge mismatch σ_{q-t} affecting SA1, built with minimum size nMOS switches, is around 85 aC, obtained using the same hypothesis than in the input modulator case. This gives rise to an input DC offset standard deviation of 31.5 nV. On the other hand, modulator SA2 is built with pMOS switches with minimum length and $W = 2$ µm, to avoid an excessive voltage drop across it. Then, since the charge mismatch increases roughly with $\sqrt{W}$ (injected charge and C_{ov} scale with W, but mismatch decrease with $\sqrt{W}$), its contribution can be estimated around 50 nV. Both of them are negligible.

In standard folded cascode amplifiers with embedded chopper demodulators another source of residual offset has to be evaluated. An offset is present between both M_9-M_{10} and M_{11}-M_{12}, which ideally carry the same current. Since this common-gate devices have usually almost minimum length and small area, this offset can be significant. Due to this, a voltage V_o is originated at the cascode transistor sources and applied to $C_{p1,2}$ and $C_{p3,4}$, which represents the parasitic capacitances at the respective nodes. Due to chopping, instead of a DC voltage, a square waveform with peak-to-peak amplitude $2V_o$ appears on the capacitances. This leads to a double effect: V_o charges and discharges capacitances, leading to an AC current, which is then demodulated by the demodulator itself; moreover, current source currents are modulated by this square voltage. The resulting offset current can be referred to the input dividing by G_m [7.8]:

$$V_{io} = \frac{4 f_{ch} C_p V_o}{G_m} + \frac{2V_o}{r_d G_m} \tag{7.51}$$

where r_d is the current source M_5, M_6 and M_7, M_8 output resistance. Monte-Carlo simulations have shown σ_{V_o} around 1.6 mV for the chosen device sizing. In addition $C_{p1,2}$ is around 100 fF, due to the large size of M_5 and M_6. Furthermore, r_d in case of M_5 and M_6 are in the order of 150 kΩ, since they carry a large current (90 µA). It turns out that this contribute is not negligible and can reach a few tens of µV, depending on the amplifier sizing. Then, the solution depicted in Fig. 7.25 has been adopted [7.8]. The boosting amplifiers establish a virtual ground on top of the parasitic capacitors. In this way, V_o is strongly reduced by the booster gain and this source of offset is reduced by three orders of magnitude (folded cascode boosting amplifiers). Offset of A_n and A_p is also

compensated by CHp and CHn. It can be also noted that the offset of A_p and A_n appears as a constant voltage on C_{p1-4}. It turns out from this estimation that the residual DC offset can be ascribed only to the input modulators.

7.4.5 Class AB control and output stage

Since the preamplifier has to drive a switched capacitor load, the output stage has to provide a significant peak current. Hypothesizing the first-order RC transient described in the previous sections, the peak current value is obtained when the sampling capacitor C_s is connected to the output and is given by:

$$I_{peak} = \frac{V_{out}}{R_{out}} \tag{7.52}$$

If $V_{out} = 0.9$ V and $R_{out} = 5$ kΩ, $I_{peak} = 180$ µA. If R_{out} is smaller, I_{peak} can clearly be even larger. A class-A output stage has to be biased with at least the current it has to provide to the load, and would turn out to be not power-efficient. For this reason, a class-AB output stage has been adopted.
The class AB control is performed by the floating V_{AB} batteries embedded into the first stage. The schematic of the class-AB mesh implementing the battery is shown in Fig. 7.26 [7.9], together with the output stage. Clearly, due to the fully differential output, two identical branches are present in the output stage. Transistors M_{AB1}-M_{13}-M_{14} and M_{AB2}-M_{15}-M_{16} form two translinear loops that fix the DC voltage of V_{op2} and V_{op1}, respectively. If $(W/L)_{16}/(W/L)_{AB2} = I_b/(I_2/2)$ and $(W/L)_{14}/(W/L)_{AB1} = I_b/(I_2/2)$, then $V_{op1} = V_{GS15}$ and $V_{op2} = V_{dd} - V_{GS13}$. This means that the output quiescent current I_q is a scaled replica

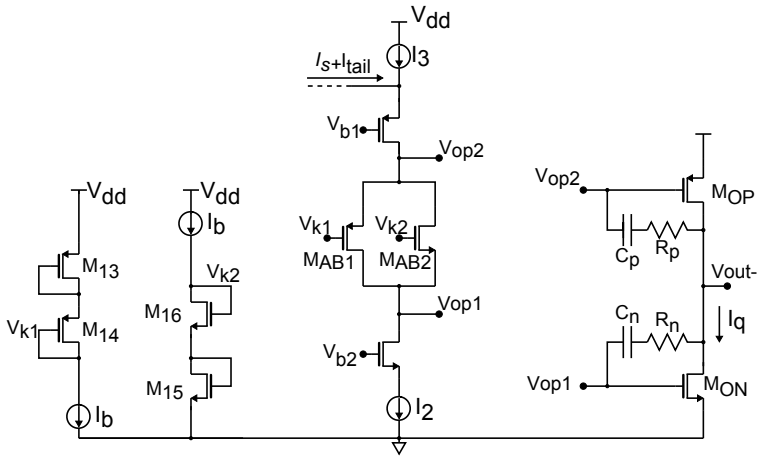

Figure 7.26: Class-AB control circuit and output stage.

of I_b and is given by $I_b \cdot (W/L)_{ON}/(W/L)_{15} = I_b \cdot (W/L)_{OP}/(W/L)_{13}$.
The DC value of V_{op1} and V_{op2} has been chosen 0.605 V and 1.065 V, respectively, in order to provide a large enough voltage headroom to the first stage cascode branches. With this choice, $V_{GSON} - V_{TH} = 160$ mV and $V_{GSOP} - V_{TH} = 260$ mV. The output swing results then to be large enough.
The control current I_b has been set to 6 µA and $I_q = 30$ µA. Finally, M_{ON} size is 0.768/0.64 with multiplicity 6 and $g_{mON} = 324$ µS and M_{OP} 1/0.5 with multplicity 6 and $g_{mOP} = 217.4$ µS. Then, the second stage transconductance G_{m2} is given by:

$$G_{m2} = g_{mON} + g_{mOP} \tag{7.53}$$

and results to be 541 µS. Transistors M_{AB1} and M_{AB2} have been sized in order to carry the same current (5 µA) when no signal I_s is applied, for symmetry reasons. This means $g_{mAB1} \approx g_{mAB2}$.
Simulations have shown an I_q variation across all corners and temperature of $\pm 30\%$, which is an acceptable value for the target application.
The preamplifier frequency compensation is achieved by means of the Miller's capacitance $C_n = C_p = 3.5$ pF. With this choice, the GBW results to be 12.5 MHz.
Right Half Plane (RHP) zeros have been compensated by means of R_n and R_p, of 8 kΩ and 12 kΩ, respectively. Their values has been chosen by means of simulations.
It should be noted that with this values the second pole, given by $G_{m2}/(C_L + C_{op})$, where C_{op} is the parasitic capacitance at the output node, is shifted to really high frequencies (720 MHz), when C_L is taken as $C_s = 120$ fF. More likely, other parasitic poles will be positioned at lower frequencies and limit the GBW. However, with $C_L = C_s$, stability is not a concern. The situation changes when the amplifier has to drive the pads as in the test-chip described here. A maximum load of 100 pF on each output terminal has been estimated. In this case, $f_{p2} = G_{m2}/(2\pi C_L) = 860$ kHz, which is lower than the GBW product of the amplifier. This clearly leads to negative phase margin. This problem has been solved adding a decoupling resistor $R_{dec} = 1.5$ kΩ in series with the pad. In this way, a zero at $2\pi R_{dec} C_L$ is introduced and the phase shift due to the pad capacitance is partially compensated and stability in all the working conditions can be ensured.
It is important also to note that at high frequencies the Miller's integrator

output impedance is given by:

$$R_{out} = \frac{1}{G_{m2}} = 1.85 \text{ k}\Omega \tag{7.54}$$

This value is low enough to properly drive the ADC input sample-and-hold circuit.
The output common-mode V_{co} of the preamplifier has to be stabilized. This is obtained by a common-mode feedback loop, which senses the output common-mode and drives the first stage in order to drive, in turn, V_{co} towards a reference voltage V_{ref}. This is possible since the second stage does not reject common mode signals, rather amplifying them. The circuit is not reported here. However, it draws a total current of 60 µA.

7.4.6 Phase generator

The necessary phases previously described have been obtained by means of a non-overlapped phase generator, build using standard logic cells, starting from a clock with frequency $2f_{ch}$. Particular care has been taken to let DEM commutation occur when chopper switches are all open. All phases are not overlapped to any of the others.

7.5 Simulations and expected performances

In this section simulation results will be shown. Measurement results are not yet available at the time this report has been written.

7.5.1 DC Offset

As described in the previous sections, HEXAGON is a chopper instrumentation amplifier. The ripple filtering is demanded to the digital part after the analog-to-digital conversion. This strategy can be adopted if the ripple amplitude does not limit too much the output swing.
Amplifier gain A_d is 13, while maximum input signal is 62 mV. Maximum allowed output differential peak voltage is 0.9 V. Then, ripple differential peak amplitude should not be larger than around 94 mV, corresponding to a maximum DC offset of 7.2 mV. To evaluate the HEXAGON DC offset, MonteCarlo runs have been performed taking into account mismatch, and DC differential output has been saved. It should be noted that here and in every simulation performed at DC, bootstrapped switches have been replaced with

ideal switches, since they work properly only in time-domain. Fig. 7.27 shows

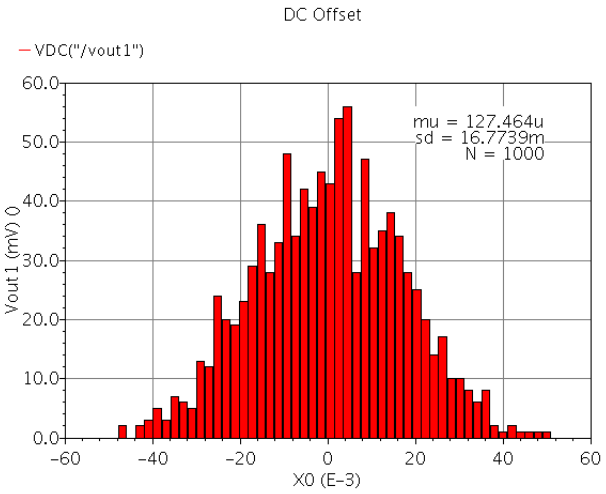

Figure 7.27: Output DC offset as obtained from 1000 MonteCarlo runs.

the output offset distribution resulting from 1000 MonteCarlo runs at T=27°C. The output offset mean value is 127.5 µV, corresponding to an input offset mean value μ_{in} of a negligible value lower than 10 µV. Output standard deviation $\sigma_o = 16.77$ mV corresponds to an input offset standard deviation $\sigma_{io} = 1.29$ mV. Then, $\pm 3\sigma_{io} = 3.87$ mV, and $\pm 5\sigma_{io} = 6.45$ mV. Therefore, since the maximum ripple amplitude results to be around 84 mV ($A_d \cdot 5\sigma_{io}$), the given specification results to be satisfied.

7.5.2 Offset

The DC residual offset is mainly due to modulator non-idealities, as widely discussed in the previous section. Accurate MonteCarlo transient simulations with zero input have been performed and output voltages have been numerically averaged over DEM period $2T_{ch}$. The residual output DC offset affecting the two channels has been obtained running 100 MonteCarlo simulations.
While mean value is decisively negligible, as expected, channel 1 output offset standard deviation $\sigma_{o-res1} = 20.36$ µV, and channel 2 output offset standard deviation $\sigma_{o-res2} = 22.34$ µV, corresponding to the input-referred standard deviations of $\sigma_{io-res1} = 1.56$ µV and $\sigma_{io-res2} = 1.72$ µV, respectively. This offset values are in line with the desired µV offset level specifications. Unfortunately, as noted in Sec. 7.4, tests performed with very simple switch structures have shown that offset introduced by charge-injection mismatch seems to be poorly modelled by the simulator. Then, the provided values are not fully reliable. An

actual offset statistic will be provided when measurements on the fabricated chip will be available.

7.5.3 Gain Matching

One of the most relevant specifications to be satisfied is the gain matching between the two channels to be achieved with the limited silicon area available. The adopted DEM techniques have been described in the previous chapter. Here, results are reported and discussed.

The distribution of the output average voltage of each channel when a 50 mV step is applied to both channels, has been obtained by 100 high accuracy MonteCarlo runs. The average gain, equal for the two channels, is 651.38/50 = 13.0276. The small discrepancy with the ideal value, 13, is due to the on-resistance of the DEM switches, equal to around 68 Ω. The gain standard deviation is 0.4920% for the first channel and 0.4919% for the second channel. They are very similar thanks to the DEM techniques.

More important is the relative gain-matching. It has been measured with the same settings and is given by $(A_{d1} - A_{d2})/[(A_{d1} + A_{d2})/2]$. Its distribution, obtained from the same MC runs, is shown in Fig. 7.28. Both process and mismatch statistics have been activated in this case to verify the effectiveness of DEM also over process variations. The relative gain mismatch standard

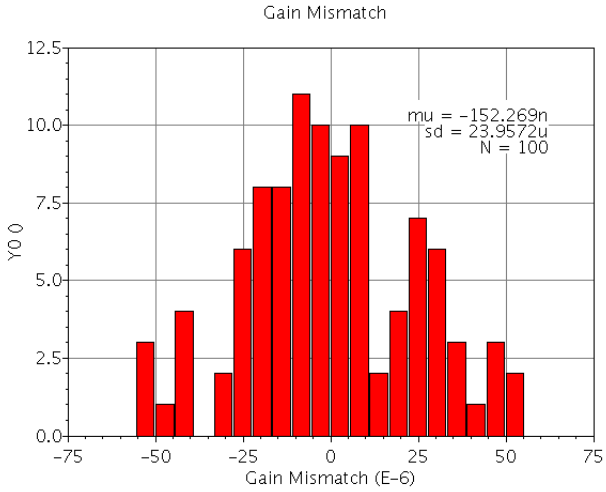

Figure 7.28: Relative gain mismatch distribution as obtained by 100 MonteCarlo runs.

deviation $\sigma_{\Delta G/\overline{G}}$ is around 25 ppm, which is a very small value. It should be noted that the specification indicated $\sigma_{\Delta G/\overline{G}} = 0.05\% = 500$ ppm. The

obtained performance is more than one order of magnitude better than what required, thanks to the DEM techniques used. It should also be noted that the residual gain-mismatch seems to be better than what expected from calculations on the DEM switches, which are apparently the most important source of gain-mismatch.

7.5.4 Noise performances

Due to the switching nature of the chopper modulation, the best way to simulate the noise performances of the amplifier is to use Spectre PNOISE simulations. The input noise PSD is shown in Fig. 7.29. Flicker noise impact at low

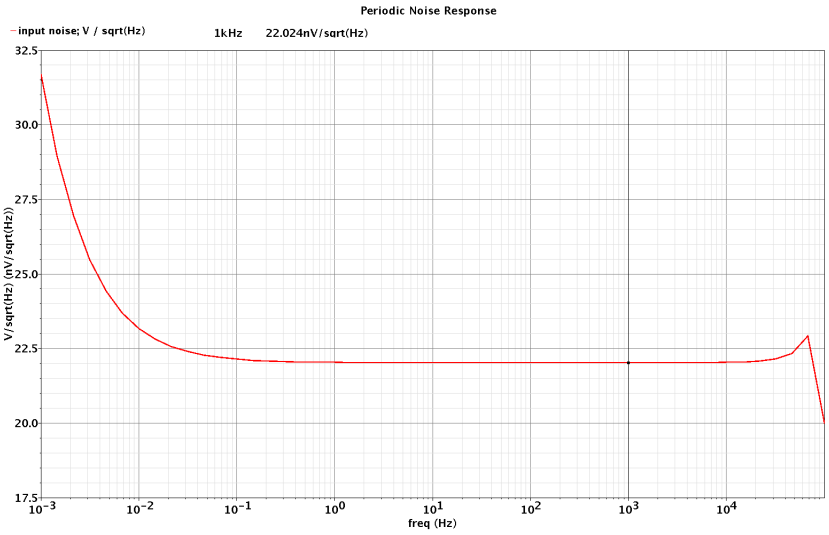

Figure 7.29: Input noise PSD of the preamplifier as obtained by a PNOISE simulation.

frequencies has been reduced by chopping, as expected. The input noise PSD is then about 22 nV/$\sqrt{\text{Hz}}$ for most frequencies in the band of interest 0-80 kHz, slightly larger than that required (20.7 nV/$\sqrt{\text{Hz}}$), for the reasons explained earlier. The corner frequency f_k is positioned slightly above 1 mHz. Although this value is not fully reliable, a very low corner frequency is expected. For what concerns the higher part of the spectrum, noise PSD is practically flat until 20 kHz, then starts to slowly increase due to the flicker spectrum. Actually, flicker PSD is moved to 200 kHz by chopper modulation, and back to 100 kHz by DEM, which can be represented as an additional modulation by a square wave varying from 0 to 1. Fig. 7.30 shows noise around DEM frequency (100 kHz). The corner frequency is around 95 kHz. The noise PSD increases only marginally up to 80 kHz.

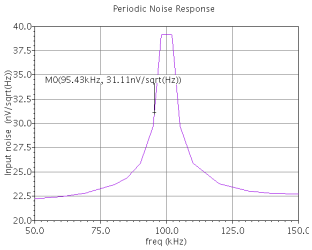

Figure 7.30: Input noise PSD around 100 kHz.

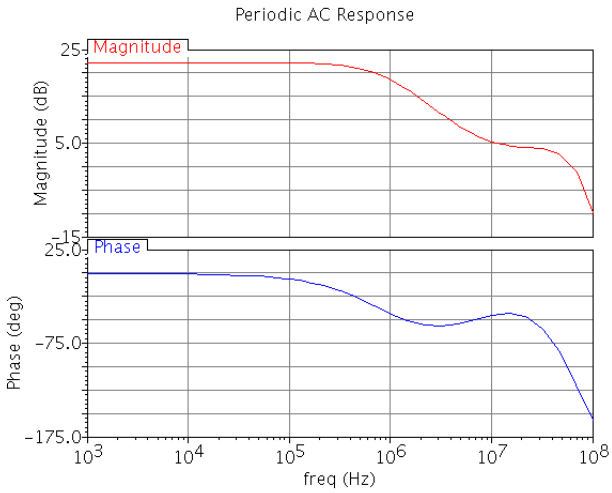

Figure 7.31: HEXAGON transfer function.

In addition, noise has been evaluated also by means of MonteCarlo AC-NOISE simulations. This is important to evaluate the common-mode noise sources contribution, e.g. current reference noise. These contributions, not present in the nominal case thanks to differential operations, could become relevant due to mismatch. The worst-case noise PSD returned by 100 AC-NOISE MonteCarlo simulations at 200 kHz is 22.3 nV/$\sqrt{\text{Hz}}$.

7.5.5 Periodic AC, linearity and crosstalk

Periodic AC response

The transfer function of the amplifier can be evaluated both by means of AC or Periodic AC analysis. However, it is preferable to use Periodic AC in order to take into account effects deriving from the switching operations. Fig. 7.31 shows the amplifier transfer function as obtained from Periodic AC simulation performed with Spectre-RF with $C_L = 1$ pF. The dominant pole is around

850 kHz. It should be observed that the transfer function response does not decrease monotonically. The contribution of two LHP zeros, located around 8.8 MHzand 17.5 MHzand originated by the zero-nulling resistors, can be identified.

Linearity

The preamplifier linearity have been evaluated by means of PSS simulations, performed with Spectre-RF. At first, THD has been evaluated at nominal conditions (no mismatch) at a given input amplitude (50 mV), at different frequencies. Fig. 7.32 shows the THD obtained at the output as a function of the sinusoidal input frequency. A proportionality to frequency can be observed.

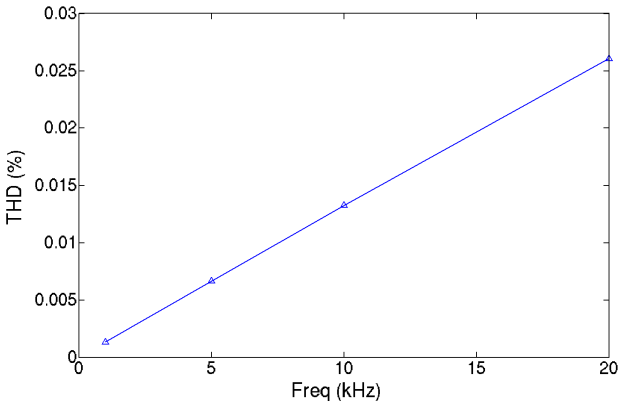

Figure 7.32: Output THD versus frequency for a given input amplitude (50 mV)

As an example, the nominal THD at 10 kHz is 0.013 % (-77.55 dB), while at 20 kHz, THD is 0.026 % (-71.7 dB). The proportionality can be explained as follows. The main nonlinearity contribution comes from the limited input range of the transconductors. However, thanks to the negative feedback, g_{in} and g_{fb} have very similar input voltages. Then, their output currents, with their harmonic content, are almost cancelled at the summing nodes. Therefore, linearity of the amplifier is increased. However, v_{fb} is not exactly equal to v_{in}. It can be approximated as:

$$v_{fb} \approx v_{in}\left(1 - \frac{1}{\beta A}\right) \tag{7.55}$$

where βA is the loop-gain of the amplifier. Since βA has a dominant pole frequency response, its value halves as frequency doubles. Then, a very similar degradation of the harmonic cancellation efficiency originates.

Nominal THD results to be very low, especially at low frequencies where higher linearity is required (see Fig. 7.8).
As previously described, amplifier non-linearity can be significantly degraded by mismatch. Therefore, several MonteCarlo runs have been performed applying at the input a signal with amplitude and frequency at their maximum values for each application, as provided by Fig. 7.8. Tab. 7.3 shows the results, including the THDs obtained by MonteCarlo simulations. In some cases, a

App.	V_{in}	f	THD spec.	THD nom.	THD max.
ABS	44.8 mV	20 kHz	-42.8 dB	-73.2 dB	-41 dB
Transm. Crank.	44.8 mV	12 kHz	-42.8 dB	-77.6 dB	-75.2 dB
BLDC	61.8 mV	1 kHz	-65.6 dB	-97.4 dB	-74.4 dB
Steering	61.8 mV	200 Hz	-75.5 dB	-111.4 dB	-72.3 dB

Table 7.3: THD results as obtained by 20 MonteCarlo runs.

significant spread of the THD can be observed, together with a degradation with respect to the ideal case. Linearity specifications are fully satisfied for Transmission, Crankshaft, BLDC applications, while for ABS and Steering applications, worst-case THD does not fully satisfies the specification. It should be pointed out that in the Steering case the average THD value obtained from 20 MonteCarlo is around -83 dB, and the maximum THD indicated in the table is largely above this value.

Cross-talk

Another important factor to be evaluated is the cross-talk occurring between the two channels. Several Periodic AC MonteCarlo runs have been performed to estimate the cross-talk occurring between the two channels. An AC signal has been applied only to a channel and the results at the output of the other channel has been measured. PAC simulations allow also the frequency dependency to be evaluated. Fig. 7.33 shows the cross-talk obtained by 20 MonteCarlo runs, defined as:

$$XT = 20 \cdot \log\left(\frac{A_{d21}}{A_{d11}}\right) \tag{7.56}$$

where A_{d11} is the gain measured between output and input of the first channel, while A_{d21} is the gain measured between output of the second channel and input of the first one. The maximum XT occurring at 20 kHz is -81.8 dB, a value that fully satisfies specifications.

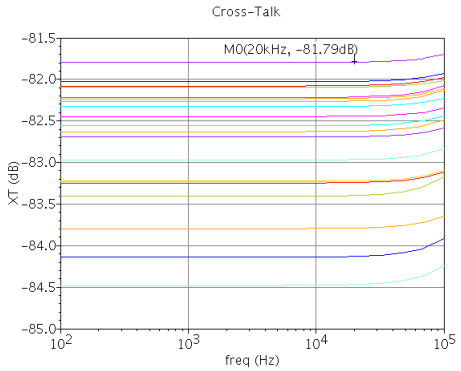

Figure 7.33: Cross-talk as obtained by 20 MonteCarlo Periodic AC runs.

7.5.6 CMRR and PSRR

The CMRR has been evaluated by means of MonteCarlo Periodic AC simulations, in order to take into account the effect of the modulations present in the circuit.

Fig. 7.34 shows the $CMRR$ obtained from 20 MonteCarlo Periodic AC runs. A dependency on the frequency can be observed. At low frequencies, $CMRR$

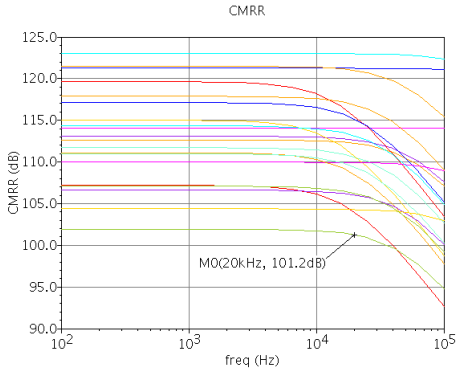

Figure 7.34: HEXAGON CMRR, as obtained from 20 MonteCarlo Periodic AC runs.

ranges from 102 to 122 dB. At 20 kHz(maximum signal frequency), the minimum $CMRR$ is then given by:

$$(CMRR)_{min} = 101.2 \ \text{dB} \tag{7.57}$$

This value is moderately high, thanks to the CFIA topology. The initial specification is then fully satisfied.

The power supply rejection ratio (PSRR) can be estimated by means of MonteCarlo Periodic AC simulations, adding a unit amplitude Periodic AC signal

to the supply.
Fig. 7.35 shows the $PSRR$ obtained from 20 MonteCarlo Periodic AC runs. Low frequency PSRR ranges from above 120 to above 160 dB, while at 20

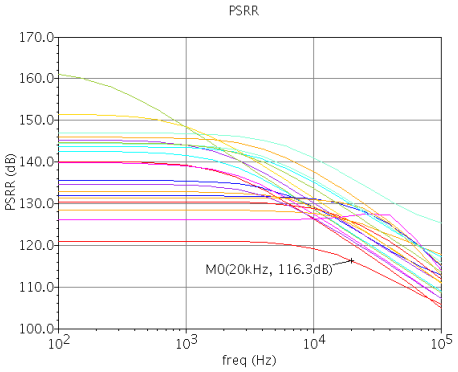

Figure 7.35: HEXAGON PSRR as obtained from 20 MonteCarlo Periodic AC simulations.

kHz (maximum signal frequency), the minimum $PSRR$ is:

$$(PSRR)_{min} = 116.3 \text{ dB} \tag{7.58}$$

which is well above the specifications.

7.5.7 Stability

Stability has been tested over corners and temperature with $C_L = 100$ pF, for $\beta = 1/13$ ($A_d = 13$). Fig. 7.36 shows the phase margin obtained for three different temperature values (-40, 27, 200°C) over all process corners. The worst-case occurs for the "fnsp" process corner at 200°C. In this case, the phase margin is slightly lower than 65°. At room temperature (27°C), the phase margin is between 70 and 72.5 °for each process corner.
As stated above, the stability has to be checked also for the CMFB loop, varying process corners, temperature and C_L. Results are shown in Fig. 7.37. The worst-case (44.5°) occurs at 200°C, for $C_L = 14$ pF, with fast-n, slow-p process corner.
Stability has also been tested with the nominal load constituted by the ADC input capacitance $C_s = 120$ fF, removing R_{dec}. This is the configuration the preamplifier is supposed to work. Differential loop worst-case phase margin of 92.8°occurs at 200°C, for fnsp process corner. CMFB worst-case phase margin of 66.7 °occurs at same temperature and corner.

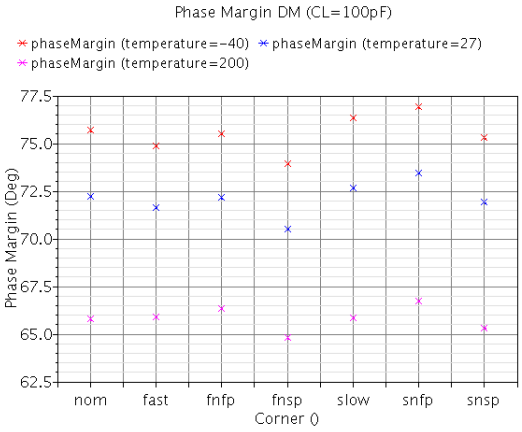

Figure 7.36: Phase margin of the differential feedback loop obtained sweeping temperature and corners, with $C_L = 100$ pF and $\beta = 1/13$.

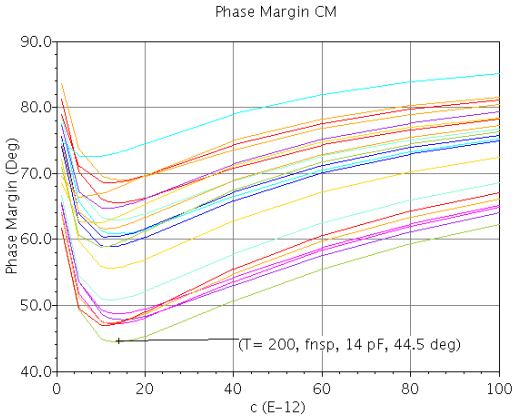

Figure 7.37: CMFB phase margins obtained from stability simulations performed sweeping C_L, corners and temperature.

7.5.8 Current Consumption

The 2-channel amplifier total current consumption is 782.2 µA, including a current reference providing all the currents necessary to the amplifier. Actually, all the biasing currents of the two channels are obtained by mirroring a single reference current of 10 µA, provided by a current reference compensated against corner and temperature. The current reference is common to both channels and draws 57.1 µA. Each channel draws 362.5 µA with an input of 0 V. If the peak output (0.9 V) is considered, the current increases up to 379.8 µA.
Tab. 7.4 reports the current consumption of each block in single and double channel configurations. The first stage gives the main contribution to the current consumption. This is especially due to the low noise and linearity specifi-

Block	Current (1 chan.) (µA)	Current (2 chan.) (µA)
First stage	230	460
Output stage	72.5	145
CMFB amplifier	58.1	116.2
Current reference		57.1
Feedback	17.3 (peak)	34.6 (peak)

Table 7.4: Current consumption of each preamplifier block.

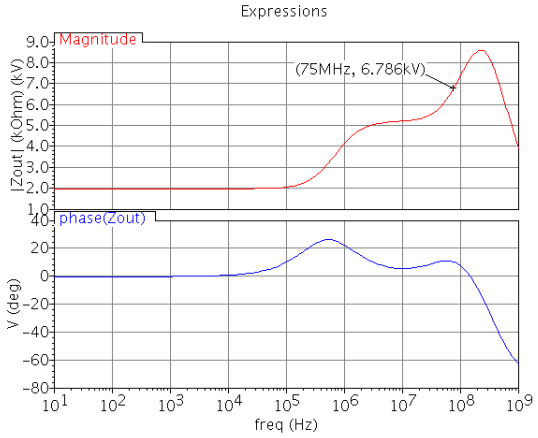

Figure 7.38: Magnitude and phase of Z_{out}.

cations. The current consumption of the CMFB amplifier is also not negligible and is due to stability considerations.

The NEF (Noise Efficiency Factor) of a single channel can be calculated taking into account the total current consumption of each channel (without considering the current reference), which is 362.5 µA. Considering $B = 900$ kHz and the input noise PSD of 22 nV/$\sqrt{\text{Hz}}$, $v_{in-rms} = 20.9$ µV. Thus, NEF results to be equal to around 16.2. It should be noted that state-of-art CFIA are characterized by NEF values around 10. In our case, the slightly larger NEF is mainly due to the source degeneration for increasing linearity.

7.5.9 Output impedance and ADC interfacing

As discussed before, output impedance at high frequencies has to be taken into account when the preamplifier is driving the ADC sample-and-hold circuit. The result is shown in Fig. 7.38, where magnitude and phase of Z_{out} are represented. The decoupling resistor has been removed. The impedance at low frequencies is given by the differential output resistance of the output stage (MOSFET r_d)

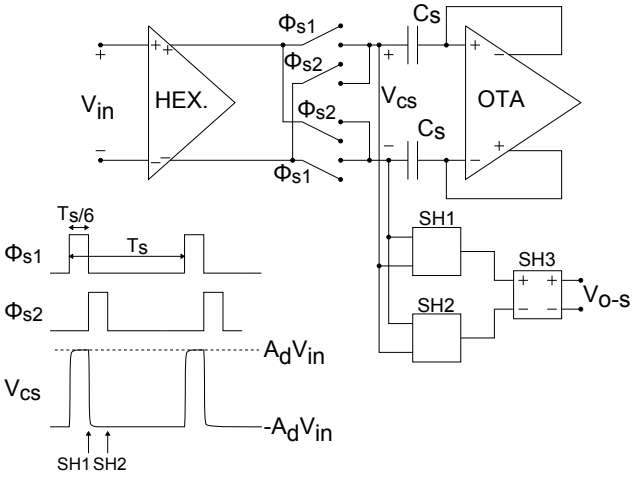

Figure 7.39: Simplified HEXAGON to ANTHILL interfacing.

divided by the gain loop (β A). However, around f_p starts to increase, reaching a plateau of 5.1 kΩ, and is given by:

$$|Z_{out}| = \frac{1}{g_{mn} + g_{mp}} \tag{7.59}$$

Then, between 20 and 200 MHz a small increase can be observed, due to parasitic poles present into the loop-gain. The high-frequency drop is due to the parasitic capacitances on the output node. At the reference frequency of 75 MHz, the differential impedance magnitude is around 5 kΩ.

The effect of the sample-and-hold has also been evaluated. The latter has been simplified as shown in Fig. 7.39. The ADC first integrator is represented by the ideal OTA block, closed in reset configuration. In this way, it has 0.9 V (output common mode) applied to both of its inputs. The working phases are also represented. SH1 and SH2 sample the waveform on the capacitors C_s at the time shown in the figure. SH3 calculates and sample their difference V_{o-s}. Actually, due to the sign inversion operated by the sampling switches, the full voltage swing appearing on C_s has to be measured, since the charge integrated by the first stage of the sigma-delta ADC will be determined by it, rather than by the peak value of V_{CS}.

For simplicity, the second channel has been omitted in the figure. The only difference consists in the delay of $T_s/3$ of the sampling phases.

It is interesting to show V_{cs} as obtained from sampling the preamplifier output when $V_{in} = 50$ mV. Fig. 7.40 shows a portion of V_{cs}, when $V_{in} = 50$ mV and $T_s = 40$ ns. The waveform settles at 662.56 mV. This value is larger than

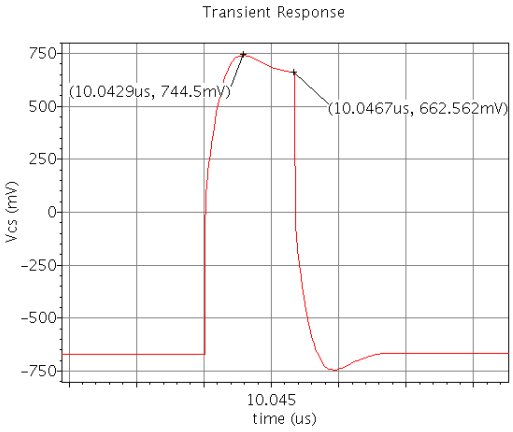

Figure 7.40: Voltage V_{cs} obtained when $V_{in} = 50$ mV.

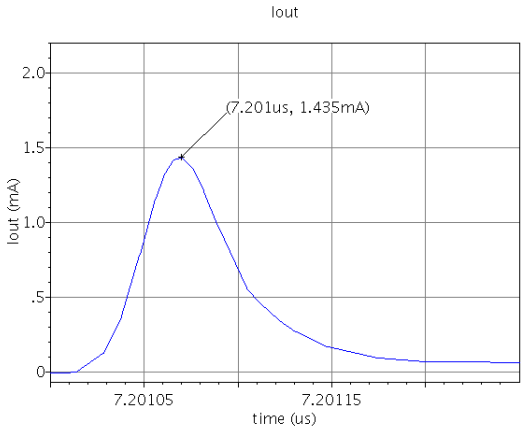

Figure 7.41: Peak current delivered by the amplifier at the sampling time.

$A_d \cdot 65$ mV for the reasons explained in Sec. 7.2.4. The slight overshoot is most likely due to the sizing of the class-AB output stage.

Gain-mismatch between the two channels can be tested evaluating the difference between V_{o-s1} and V_{o-s2}, where V_{os-1} and V_{os-2} are the output of SH3 for the two channels. MonteCarlo simulations, performed using a VerilogA description of OTA, ideal sampling switches and library components for C_s, have highlighted a negligible mean value and a standard deviation around 400 ppm. It is more than one order of magnitude worse than in the case of output not being sampled. This is mainly due to the mismatch of the output time-constants, as explained earlier. However, the gain-mismatch seems to be still acceptable. It is interesting also to report the peak current delivered by the class-AB output, shown in Fig. 7.41. The peak differential output current is 1.435 mA.

7.5.10 Benchmark

Tab. 7.5 shows a comparison of the proposed amplifier with similar solutions proposed in the literature. The supply current of this work makes reference to

	This work	Fan [7.10]	Wu [7.7]	Pertijs [7.11]	Sakunia [7.12]
Year	2012	2012	2011	2011	2011
Input PSD ($nV/\sqrt{Hz}$)	22	21	17	27	28
Supply current (µA)	362.5	143	290	1700	480
F ($S_v^2 \cdot I_s$) nV^2mA	157.5	63	83.8	1239	376
Gain error	0.0025% (σ)	0.53 %	0.06 %	0.1%	0.04 %
Area (mm^2)	0.07 (active area)	1.8	5	2.5	1.48

Table 7.5: Performance comparison.

the current of a single channel included the current reference contribution.
It can be observed that a very high gain matching between two channels is obtained with a very small amount of active silicon area. Power efficiency of the amplifier does not hit the top of the state-of-art due to the THD and robustness requirements, as widely explained in previous sections.

7.6 Layout and post-layout simulations

The layout of HEXAGON has been carried out trying to minimize parasitic effects leading to an increase of the systematic offset or to a systematic gain-mismatch. Clock shielding has been used wherever necessary, in order to avoid unbalanced charge injection to sensitive nodes. An high degree of symmetry between the layout of the two channels has been obtained, in order to match interconnections, especially signal and clock lines. In the followings few significant parts of the layout will be shown together with the results of post-layout simulations.

7.6.1 Modulator layout

Input modulator layout should be carried on with particular care, since charge injection and clock feedthrough mismatch occurring in this elements translates into additional residual offset.
Fig. 7.42 shows the layout of the modulators SA1b1. The ground (GND) path has been drawn with METAL1, while the signal paths (out1 and out2) with METAL2 and METAL3 layers. By this way, chopper phases phi1 and phi2,

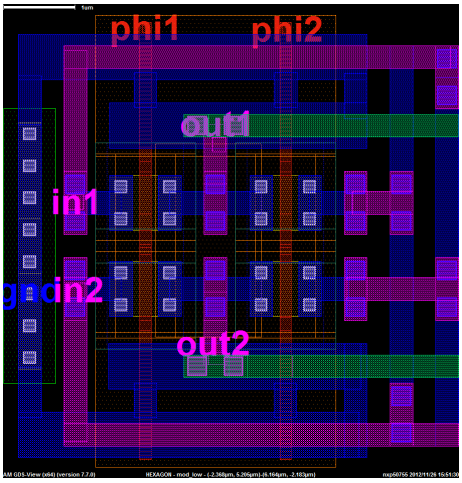

Figure 7.42: Layout of modulators SA1b1.

drawn with POLY layer, are effectively shielded from the signal. By this way, the parasitic C_{dg} capacitance between chopper phases and signal paths has been strongly reduced. Shielding by means of ground paths has been used also between signal lines of different channels to reduce risks of cross-talk.

7.6.2 HEXAGON layout

Fig. 7.43 shows the 2-channels preamplifier layout. The preamplifier size, including the current reference, is 290x250 μm^2, corresponding to an area of 0.0725 mm^2. The symmetric structure has been chosen to make as similar as possible the interconnections. The non-overlapped phase generator is also shown. Its layout has been automatically drawn by means of Encounter Place&Route to minimize its area.
The second stage occupies the largest area portion due to the compensating capacitors. The bootstrapped switches also occupy a significant area portion. This is due to the bootstrapping capacitance (2 pF).
However, the overall area devoted to the 2-channel preamplifier is very small if compared with solutions provided in the literature. It should be noted on the other hand that such a small area is achievable thanks to the choice of digital ripple filtering.
Finally, the complete HEXAGON layout is shown in Fig. 7.44.

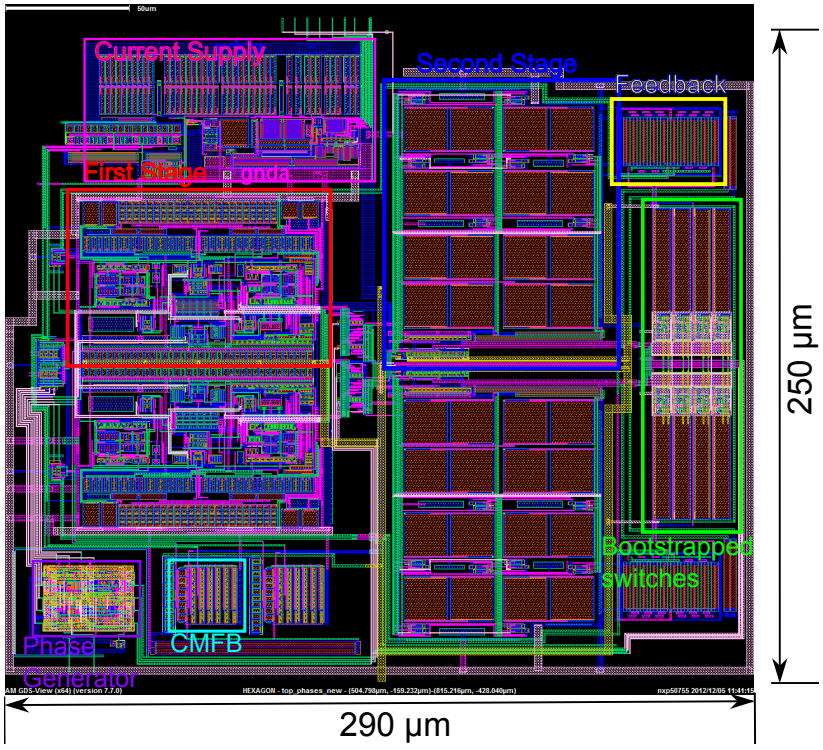

Figure 7.43: 2-channels preamplifier layout.

7.6.3 Post-layout simulations

Post-layout extraction has been performed to estimate the effects of parasitic R and C originated by layout interconnections.
The results are summarized in Tab. 7.6. V_{o1} and V_{o2} is the input-referred offset on the 2 channels. Parasitics introduced by the layout seem not to significantly

Specification	Value
V_{o1}	-414 nV
V_{o2}	-614 nV
Gain-mismatch	less than 1 ppm

Table 7.6: Main performances simulated after post-layout extraction.

impact the amplifier critical performances.

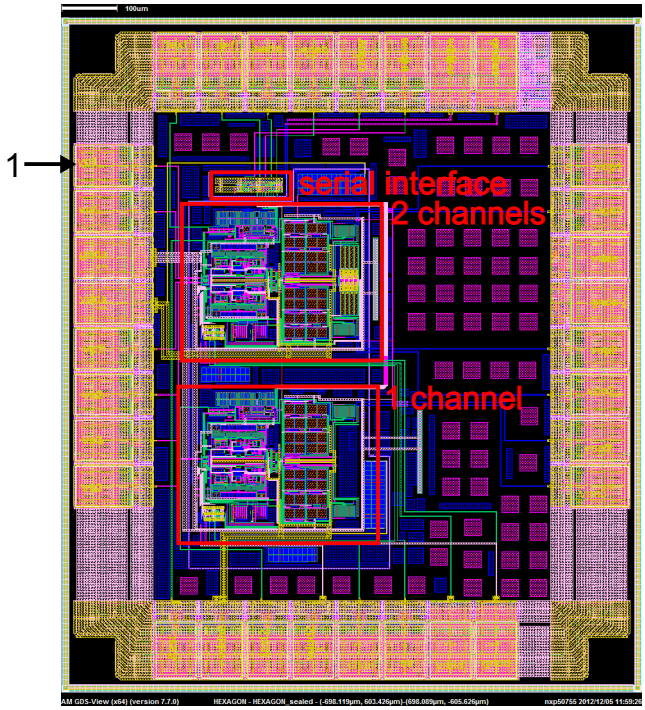

Figure 7.44: HEXAGON layout.

7.7 Conclusions and future developments

In this chapter the design of a 2-channels high accuracy preamplifier for AMR sensor bridges has been discussed. The preamplifier has to be embedded into a multi-purpose application independent front-end, prior to a sigma-delta ADC. Therefore, a challenging set of specifications had to be satisfied, including low noise and low offset, linearity and gain-matching between the two channels with a very small silicon area (less than 0.1 mm^2).

A chopper modulated current-feedback instrumentation amplifier, employing dynamic element matching between the 2 channels to achieve the required gain-mismatch, has been designed. Input noise PSD is 22 $nV/\sqrt{Hz}$, while estimated input offset results to be lower than 5 µV. Offset ripple filtering is not provided by the preamplifier and is demanded to the digital part following the ADC. Particularly significant is the gain-matching between the two channels: the standard deviation has been estimated by means of MonteCarlo simulations to be around 25 ppm. To achieve such a low mismatch with very small impact on the silicon area, dynamic element matching techniques have been employed. Actually, the total active area of the 2-channels preamplifier is around 0.07 mm^2.

Particular attention has been also devoted to ensure robustness of the preamplifier when large temperature variations (-40 to 200° C) are considered, over all process corners. This is paid especially in terms of power efficiency in reducing input noise PSD, as explained in the previous sections.
A class-AB output stage has been adopted to deliver the peak current required by the sample-and-hold circuit of the ADC (around 800 µA).
A test-chip including the 2-channels preamplifier together with a single-channel version, build as a replica of the former with a channel disabled, and a serial interface for configuration has been taped-out.
The total current consumption of the 2-channel preamplifier is around 780 µA when 0 V input is applied.
The amplifier results to be favourably comparable with other solutions in the literature but achieves a better gain matching with a very small silicon area.

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Conclusions

This thesis dealt with the design of high accuracy instrumentation amplifiers for MEMS sensor interfacing. The main research activity described was the design of a low offset, low noise instrumentation amplifier for MEMS thermal flow sensor reading. Since low frequency filtering was involved, a chapter dealing with optimization of low frequency G_mC filters has been included. Finally, the research activity carried out at NXP Semiconductors, dealing with the design of a multi-channel interface for magnetic sensors has been described.

The instrumentation amplifier has been designed using chopper modulation to achieve very low input offset. Besides, a novel port-swapping technique has been introduced, in order to improve the gain accuracy of the proposed amplifier ($\pm 0.2\%$) and increase the input impedance when chopper modulation is applied. Moreover, a narrow bandwidth filtering (200 Hz) has been implemented in the same amplifier in order to limit the output noise bandwidth. The total input noise, 20 nV/$\sqrt{\text{Hz}}$, has been obtained with a total current consumption of 170 µA from a 3.3 V source. The simulations carried out to confirm the effectiveness of the proposed approach have shown that the implemented amplifier is favourably comparable with other solution of the state-of-art.

The layout of the instrumentation amplifier has been carried out and after proper verifications has been included into a complete system-on-chip including also a 10-bit programmable heater driver and other functional blocks, such as an oscillator and a current source. The layout has been sent for production and further measurements to a foundry.

To properly optimize the instrumentation amplifier, concepts about low frequency filters have been investigated by means of automatic optimum sizing MATLAB routines, described in this thesis. The routines have proven efficient in providing useful design hints about low frequency G_mC integrators

sizing. The precision has been also improved up to an error of 5% on the target specifications, using a semi-analytical approach and moderately advanced MOS models.

Finally, the instrumentation amplifier designed during the internship carried out at NXP Semiconductors (NL) has been targeted to achieve a very high channel-gain matching, with a very small silicon area. A relative gain error between two channels of 25 ppm has been achieved by means of dynamic element matching. This technique has also allowed the silicon area to be limited to around 0.07 mm^2 for a 2-channel instrumentation amplifier.